

B450 AORUS PRO WIFI

PAGE **TITLE** **Revision : 1.1**

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04	CPU DDR4 MEMORY
05	CPU CONTROL
06	CPU GFX, GPP, SB, GND
07	CPU ACPI/GPIO/USB/AUDIO
08	CPU POWER & GND
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10	DDR4 CHANNEL A
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12	PM CLK, SPI, MISC
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16	PCI EXPRESS x16
17	HDMI , DVI
18	IT8688CX , TPM
19	F_USB30 , R_USB30 , F_USB20
20	A_VDD1V8
21	ALC1220 CODEC
22	AUDIO JACK
23	POWER SEQUENCE , A_VDDP
24	PWM SL95712
25	VCORE MOS , VCORE_SOC MOS

[illegible]

Model Name:B450 AORUS PRO WIFI

Component value change history

Version: 1.1


P-Code: U98126-0

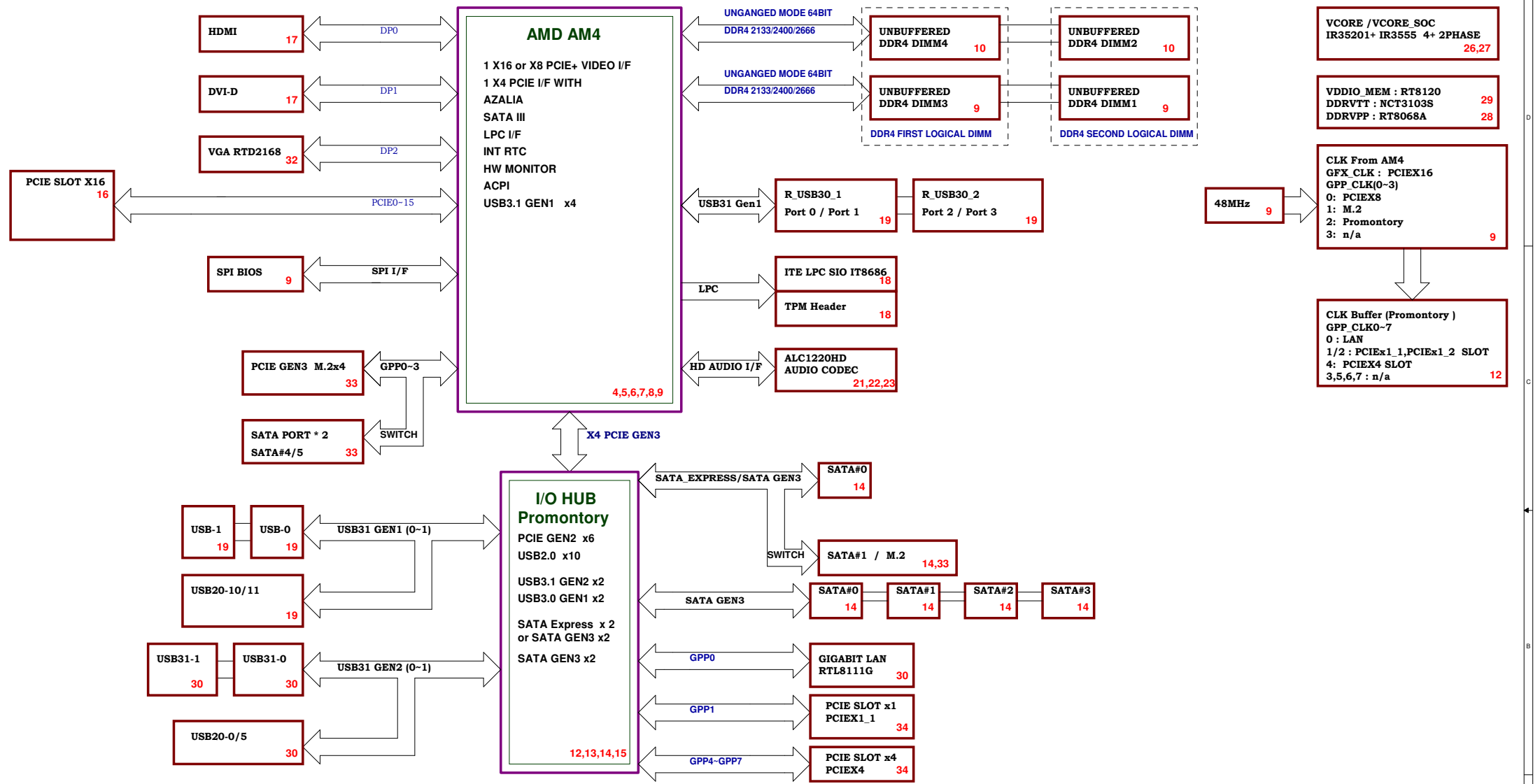
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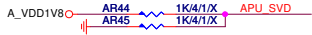
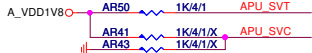
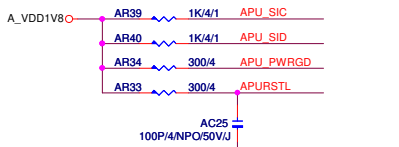
Circuit or PCB layout change for next version

[illegible]

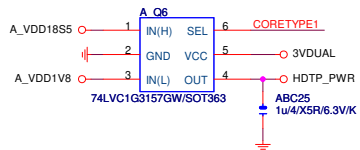
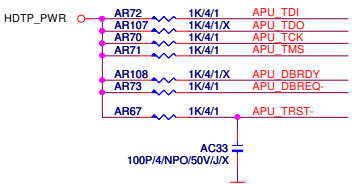
<https://vinafix.com>

			
BOM & PCB HISTORY			
Title			
Size	Document Number	Rev	
Custom	B450 AORUS PRO WIFI	1.1	
Date:	Wednesday, August 19, 2020	Sheet 2 of	B450 AORUS PRO





SVC	SVD	Boot voltage
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



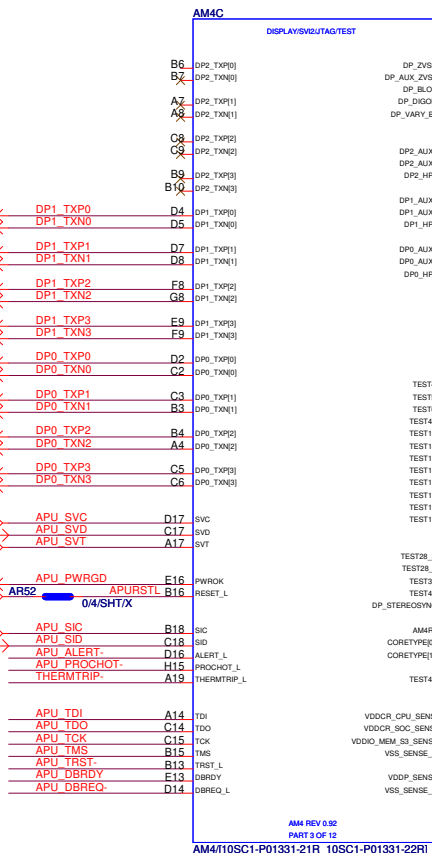
DVI

HDMI

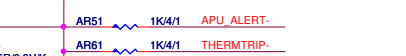
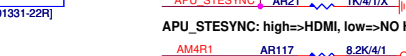
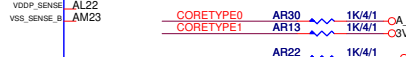
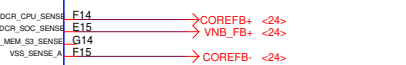
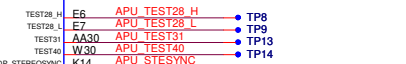
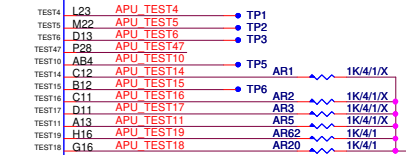
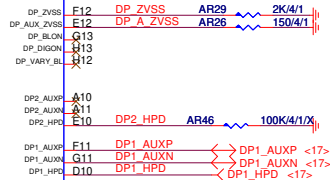
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<18>

<18>



Placed within 1500 mils from APU



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CORETYPE 1	CORETYPE 0	Family / Model Numbers	AM4 APU TYPE
0 BR	0	Family 15 h / Models 60 h-6 Fh	TYPE 0
0 ST	1	Reserved	TYPE 1
1 ZP	0	Family 17 h / Models 00 h-0 Fh	TYPE 2
1 RV	1	Family 17 h / Models 10 h-1 Fh	TYPE 3

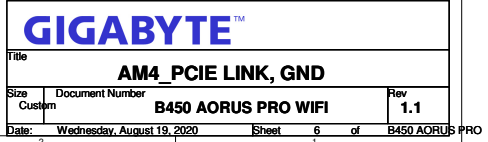
GIGABYTE

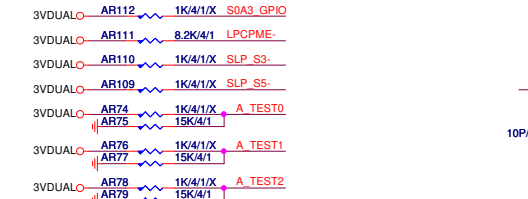
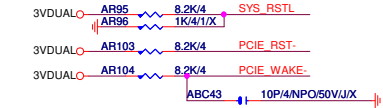
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Size: Custom Document Number: **B450 AORUS PRO WIFI** Rev: **1.1**

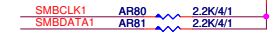
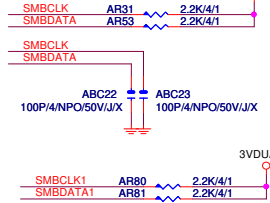
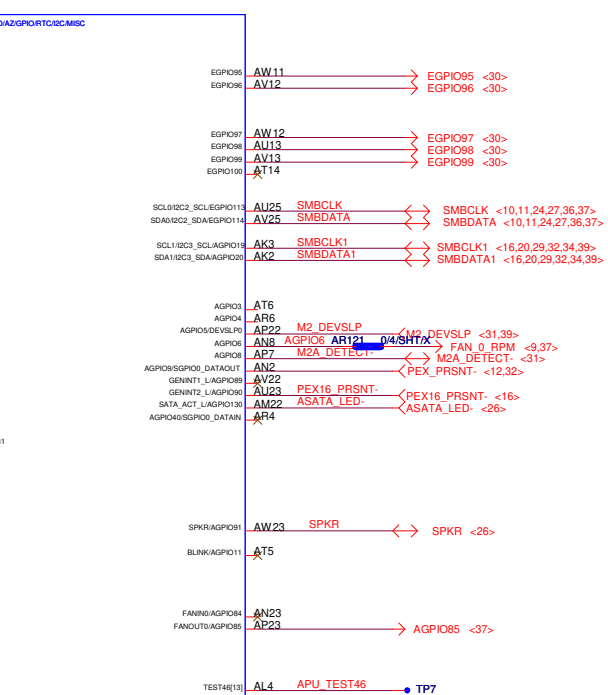
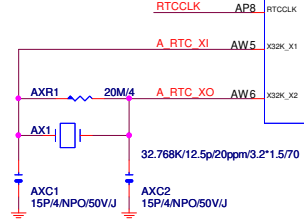
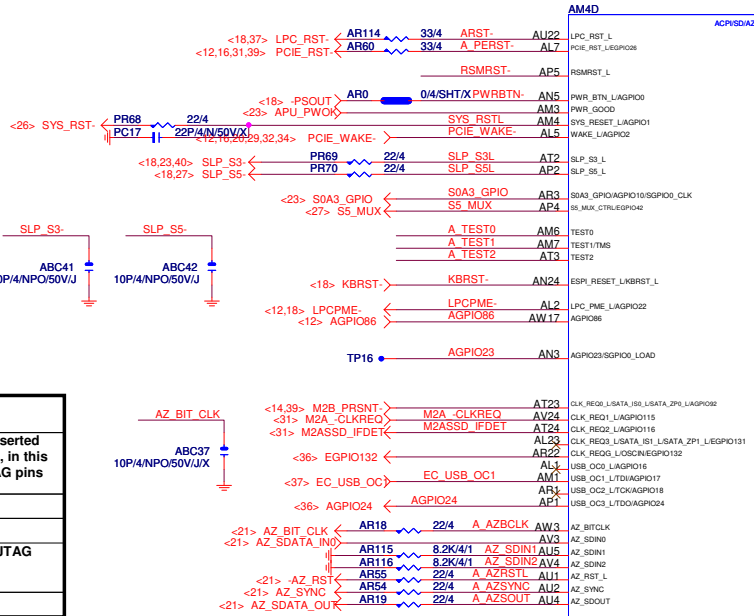
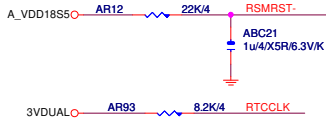
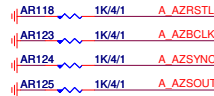
Date: Wednesday, August 19, 2020 Sheet: 5 of B450 AORUS PRO

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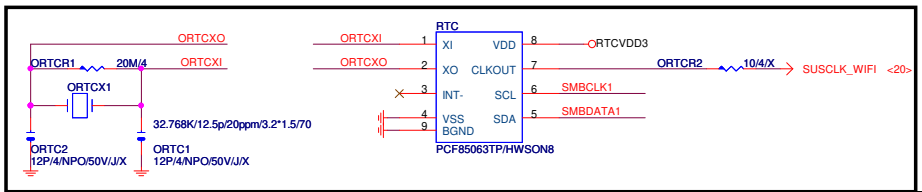
Internal Debug Only			
TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.



	LPC_CLK0	LPC_CLK1	AGPIO3	RTC_CLK	LFRAME_L	SYS_RST#	SPI_CLK (ZP)
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48MHz crystal clock and generate both internal and external clocks (DEFAULT)	Enhanced reset logic (for quicker S5 S5 resume) (DEFAULT)	Coin battery is on board. (DEFAULT)	SPI ROM (DEFAULT)	normal reset mode (DEFAULT)	Use 48MHz crystal clock and generate both internal and external clocks (DEFAULT)
PULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)	Use 100MHz PCIE clock as reference clock and generate internal clocks only	Default to traditional reset logic (DEFAULT)	Coin battery is not on board. (DEFAULT)	LPC ROM	short reset mode	Use 100MHz PCIE clock as reference clock and generate internal clocks only

CP/ST DIE ONLY
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ZP DIE ONLY

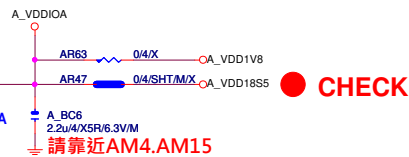
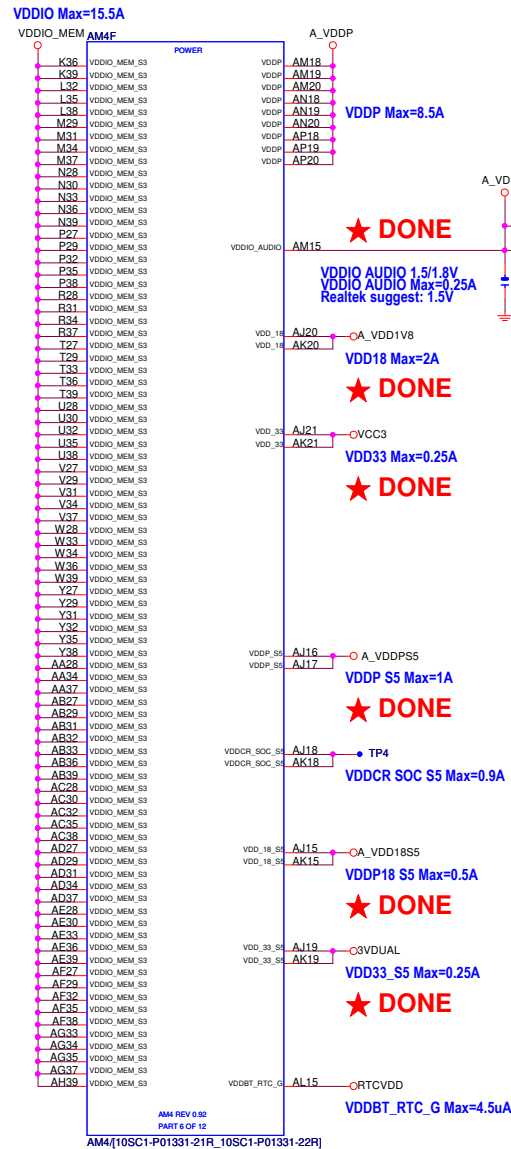


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AM4 MISC

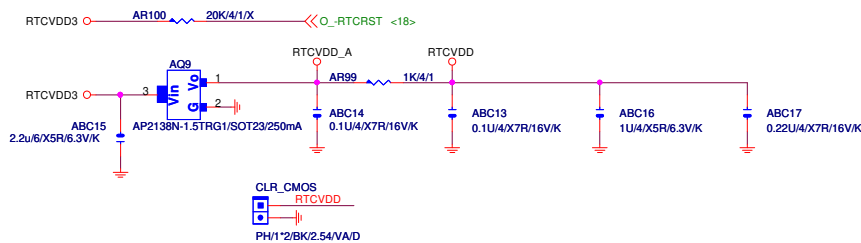
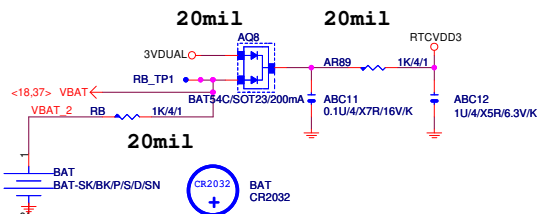
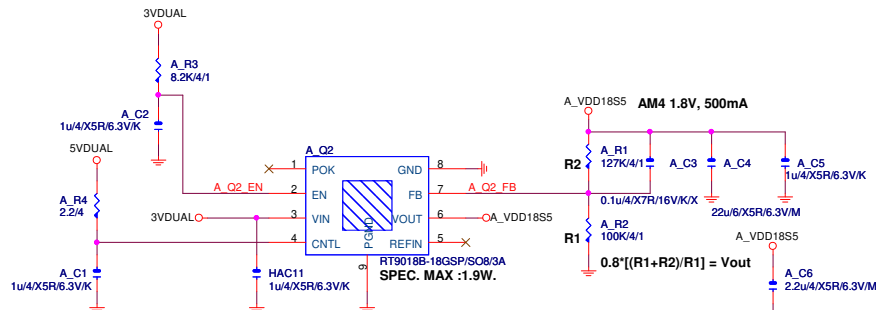
Size Custom Document Number B450 AORUS PRO WIFI Rev 1.1

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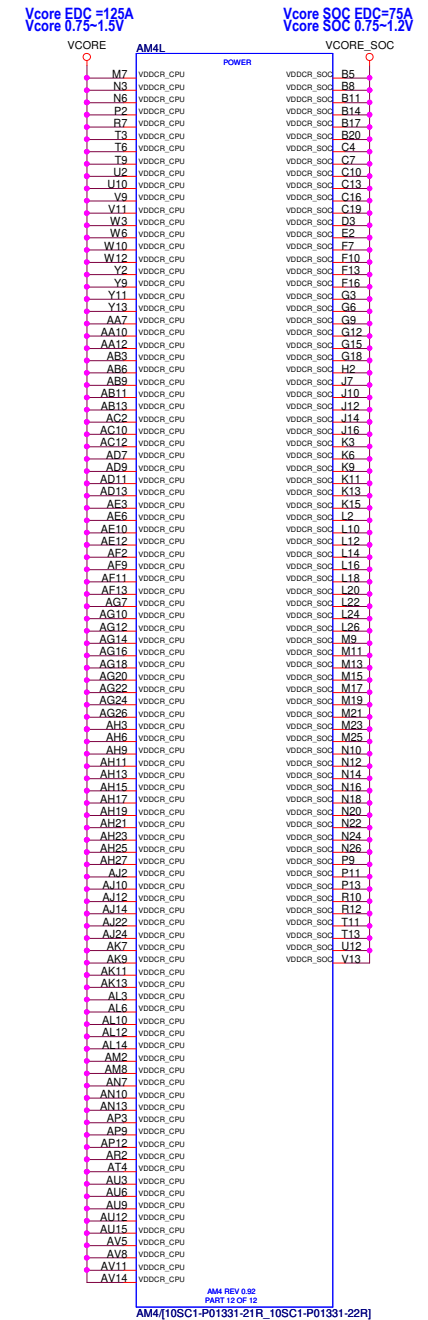


AM4 1.5V, 250mA (A_V15S5)
A_Q1 改接A_VDD18S5 for VDDIO_AUDIO

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CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL
NOT ADD ICT FOR RTCVDD PIN	



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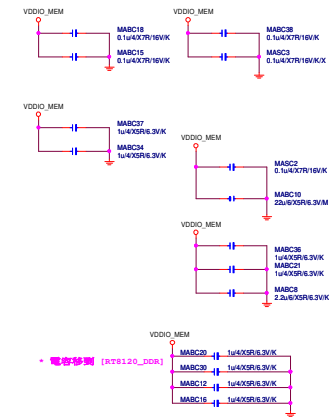
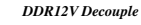
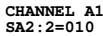
CPU POWER & GND			
Size	Document Number	Rev	
Custom	B450 AORUS PRO WIFI	1.1	
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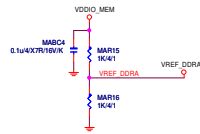
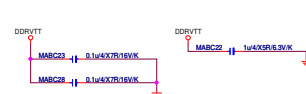


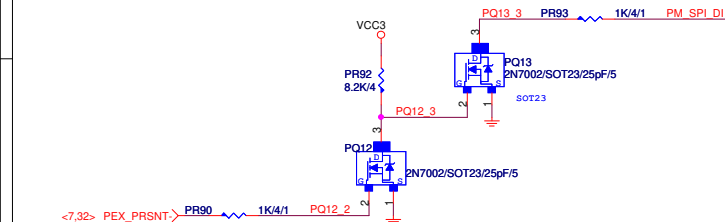


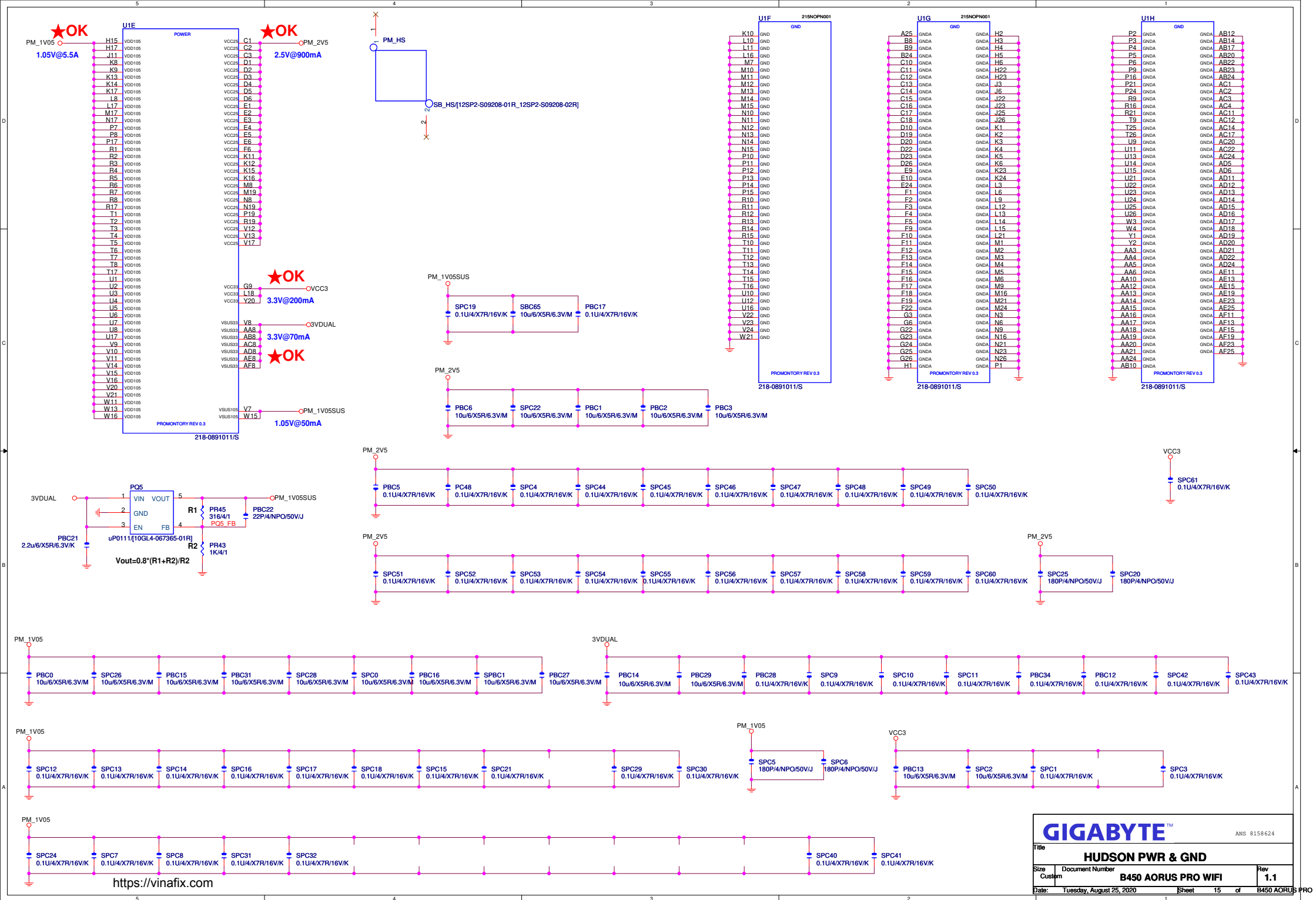
CHANNEL A0
SA2:0=000

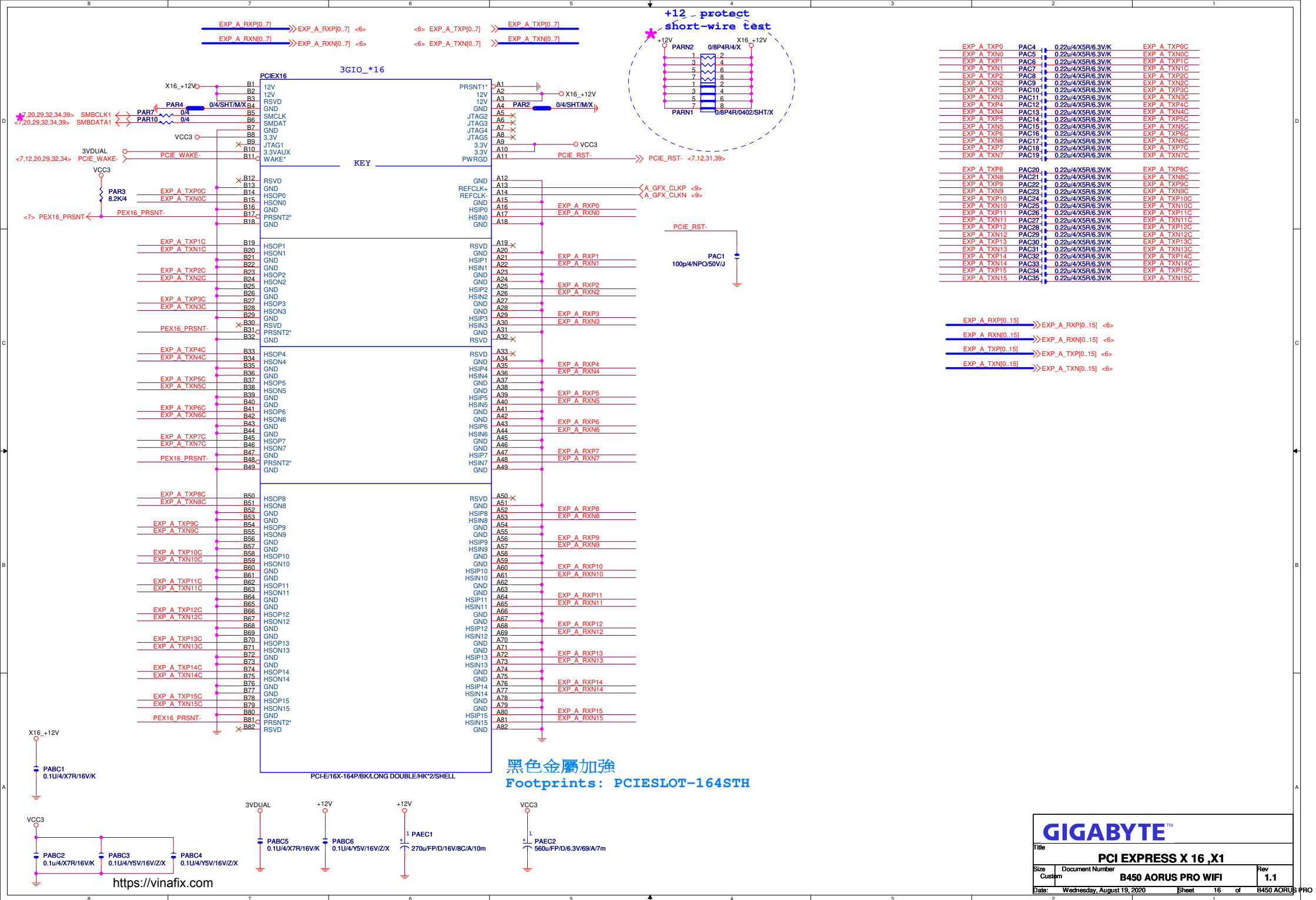


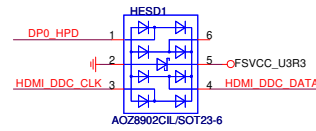
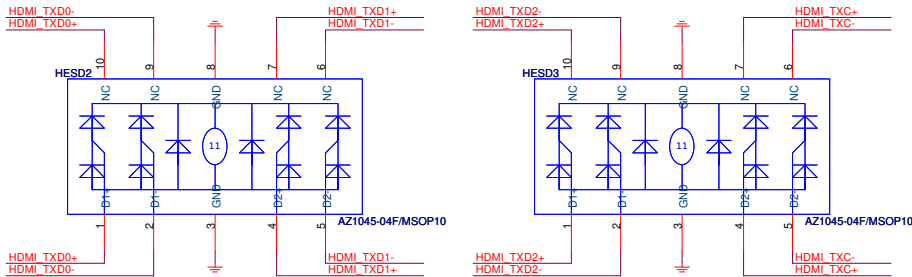
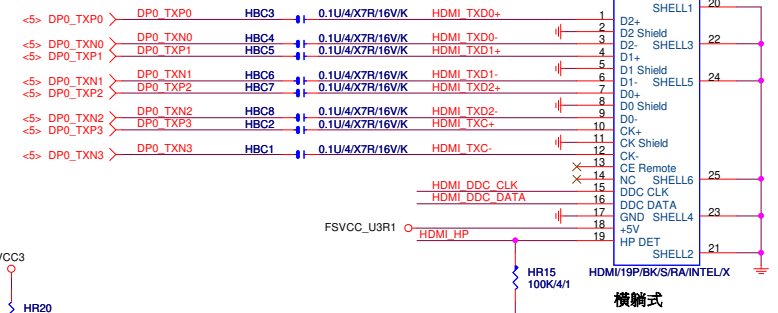
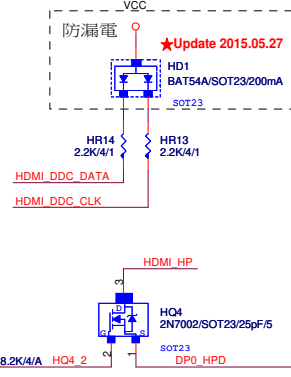
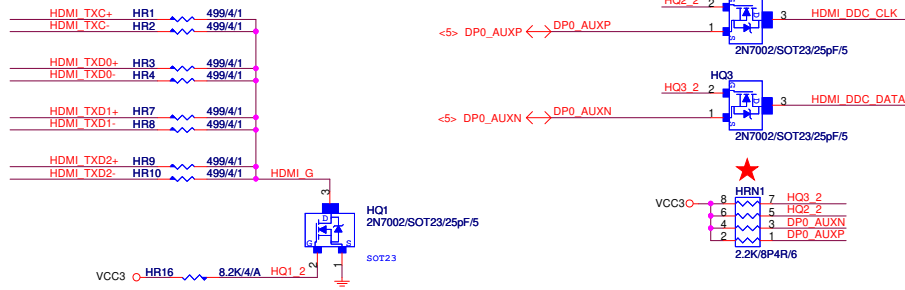
DDRVTT Decouple









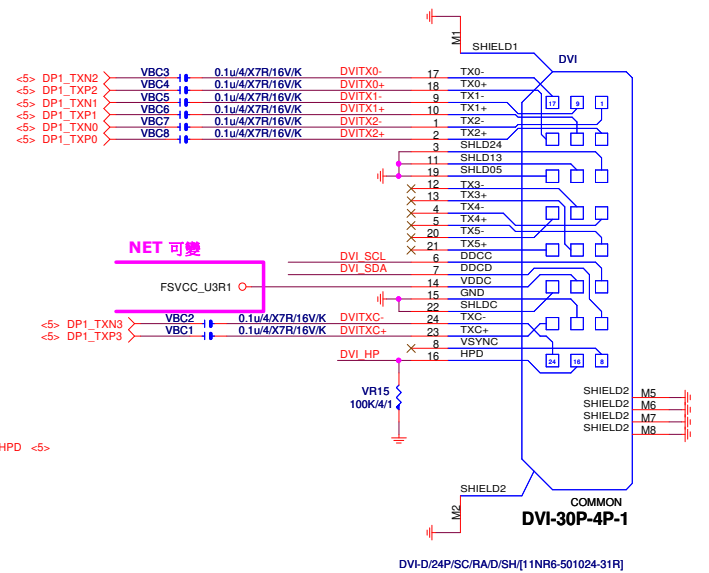
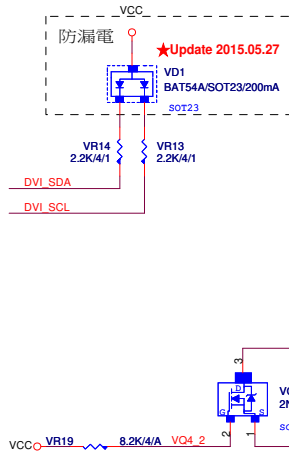
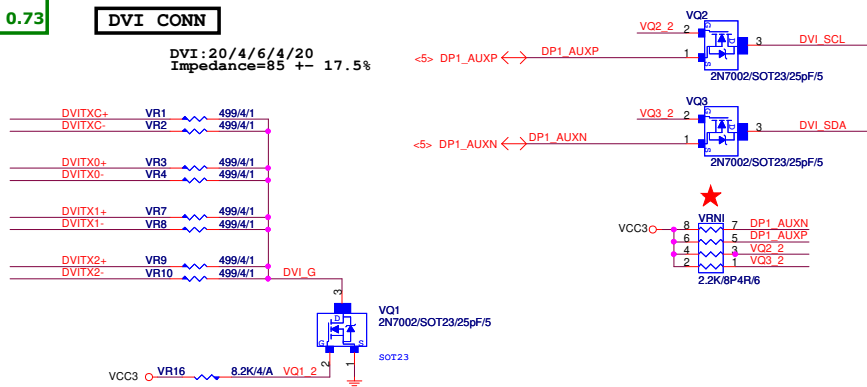


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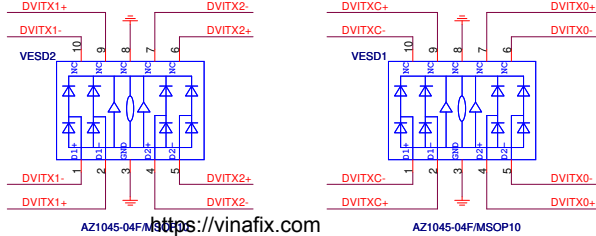
Rev: 0.73

DVI CONN

DVI :20/4/6/4/20
Impedance=85 +- 17.5%

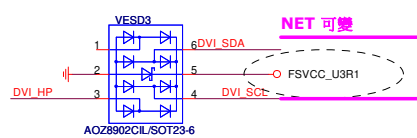


Close to connector



NET 可變

Close to connector



NET 可變

平躺式 DVI-D



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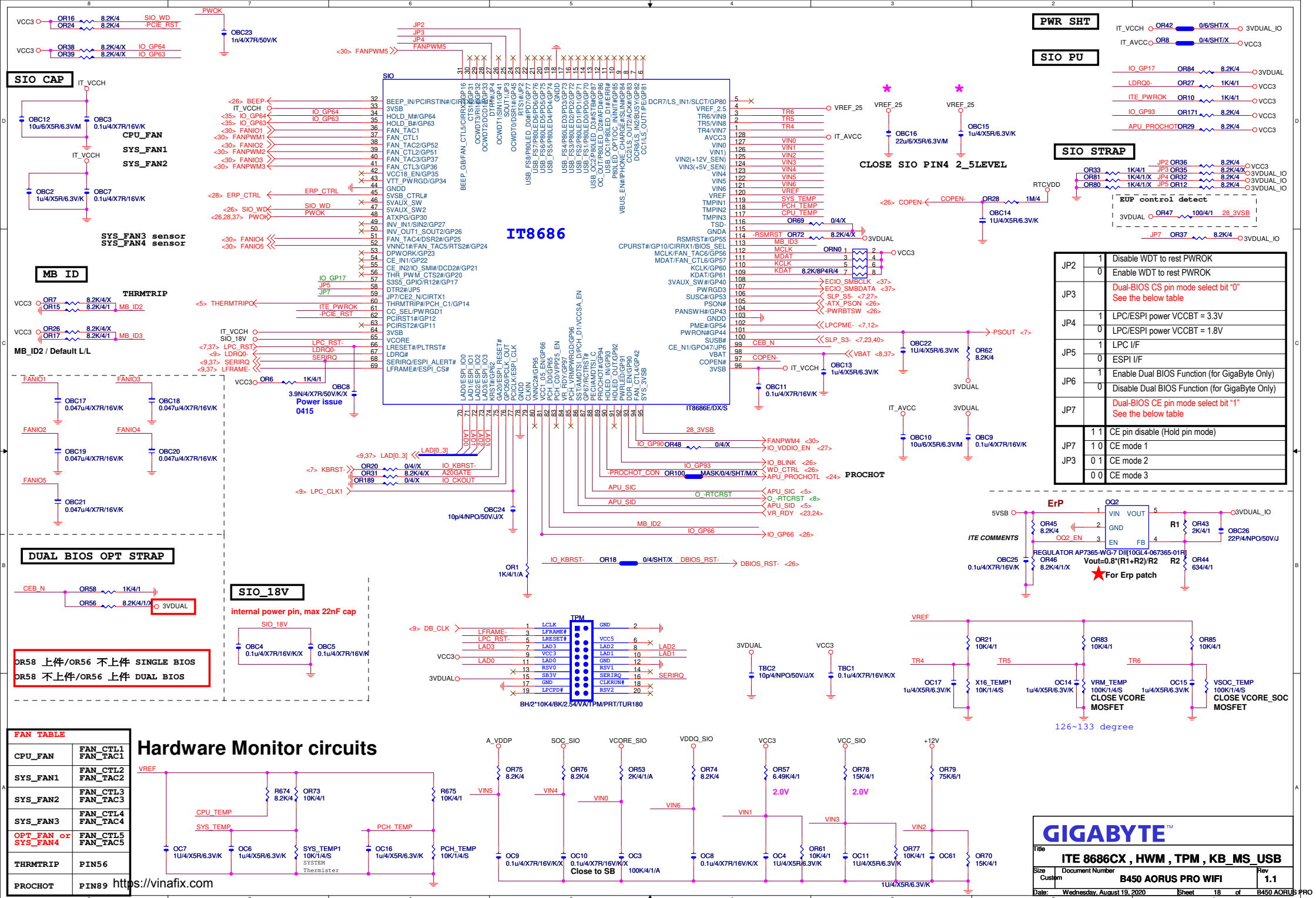
HDMI 2.0

Document Number: **B450 AORUS PRO WIFI**

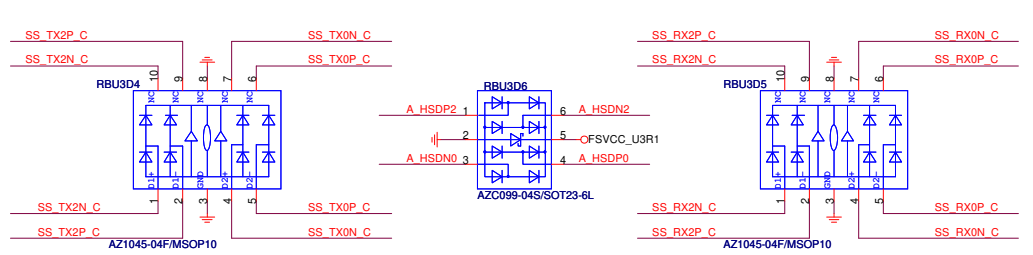
Rev: **1.1**

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REAR SIDE USB30

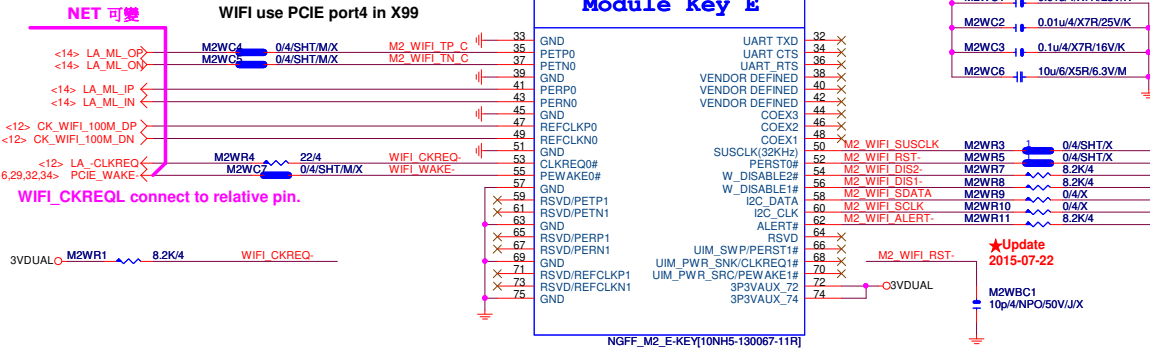


Rev: 0.2

請選擇適用的USBport :
SOC/UD7/UD5/G1/G7 : USB4
;UD3/G5:USB6

PCIE:15/4/4/15(breakout min 8/4/4/4/8)
外層Impedance=85 +- 17.5%

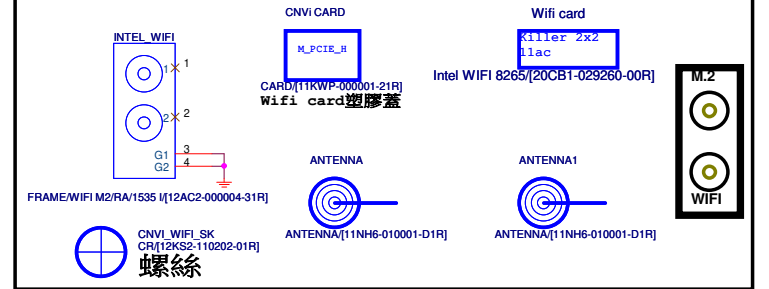
PCIE:15/4/4/15(breakout min 8/4/4/4/8)
內層Impedance=85 +- 12%



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★Update 2015-02-11

一套WIFI MODULE包含外框+WIFI CARD+天線



Footprint Notice.

★Update
2015-07-22
★Footprint
for 直立式
SMD:
WIFI-EKEY

Footprint Notice.

★Update
2015-07-22
★Footprint for
橫躺式SMD: NGFF-E-75P-2

兩片式WIFI金屬殼改為單件式
Layout Library : wifi-ekey-module-1
Tiptop P/N : 12AC2-000004-31R

REV: 0.4

A VDD1V8

CHOKE與CAP料號可變

$I_L=1u$
 $DCR=3.2\text{ mohm}$
 $I_{sat}=18A$
 $I_{dc}=15A$

VPP CAP

* 大電容 $\times 0$
22u*1PCS

A VDDPS5

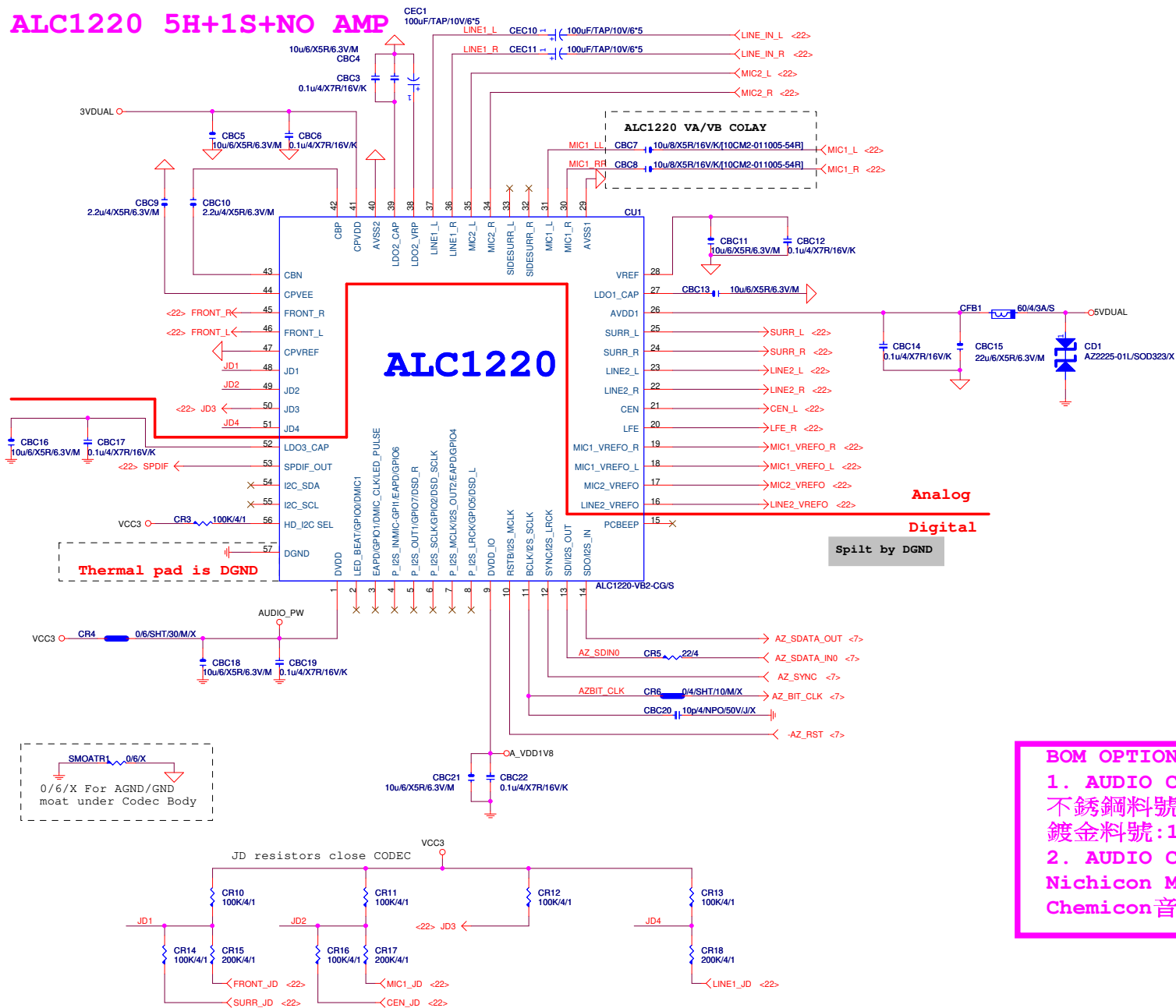
【技術通報R&D技術通報156】
RT9018 (RICHTEK) 與NCT3730 (NUVOTON),
EM5103GE (EMC) 做共用, 針對PIN7 (FB) 分壓阻值部份
(R1/R2) 須做修改為100K以上電阻值

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FAN, A_VDD1V8

Size Custom B450 AORUS PRO WIFI Rev 1.1
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ALC1220 5H+1S+NO AMP



LAYOUT注意: 螺絲孔下GND方式

1. MH1下DGND

2. MH2一律改為Isolate

MH1

DGND

MH2

Isolate

LAYOUT注意: 是否要加?

AGND切割線

音效區域印刷

BOM OPTION :

1. AUDIO CONNECT

不銹鋼料號: 11NR6-403025-A3R

鍍金料號: 11NR6-403025-92R

2. AUDIO CAP

Nichicon MW 音效電容 : 11CE1-651000-12R

Chemicon 音效電容 : 11CE2-651000-05R

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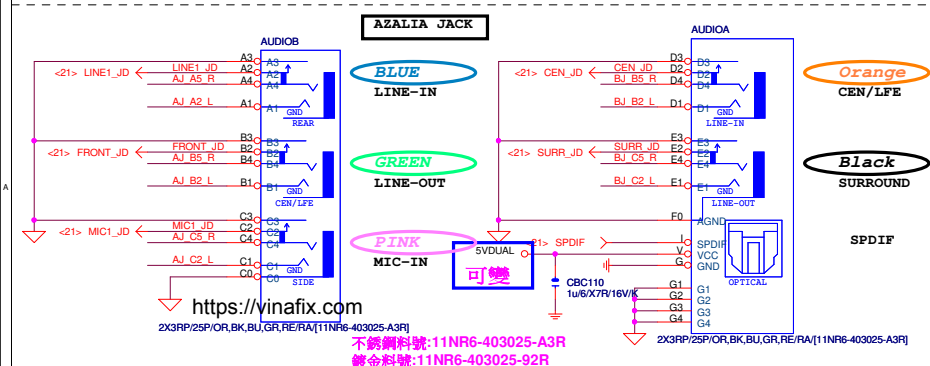
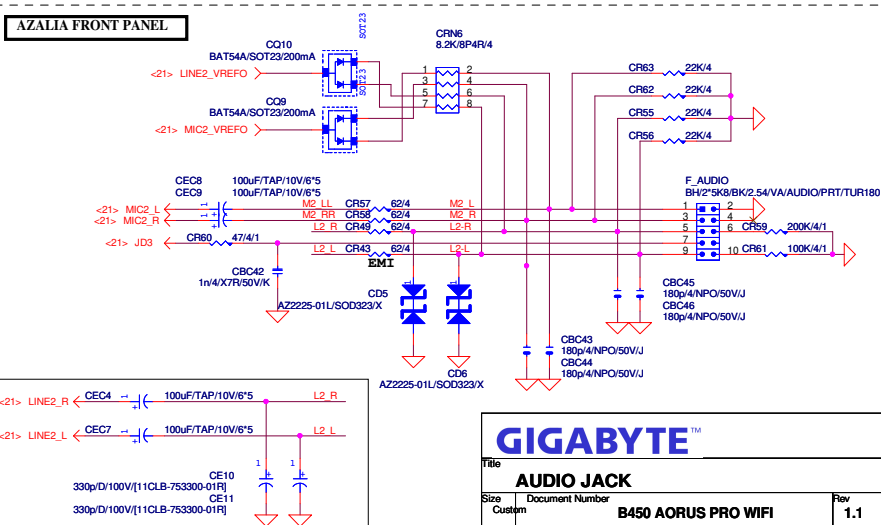
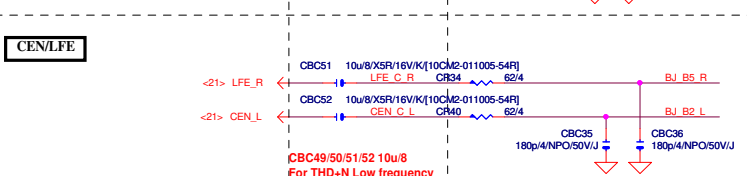
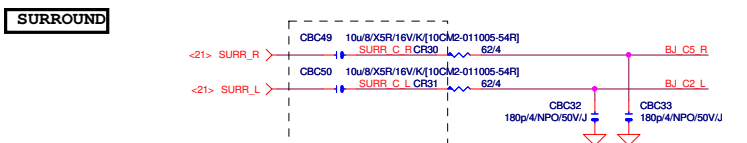
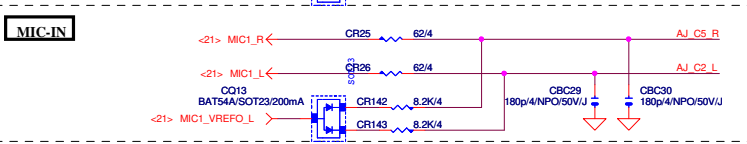
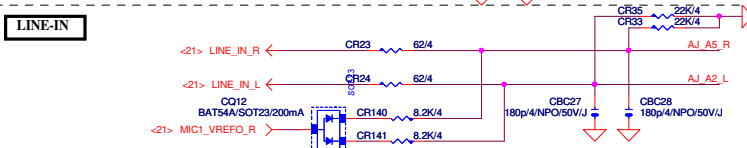
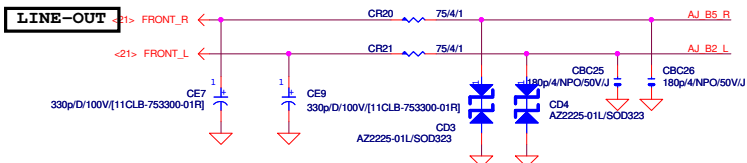
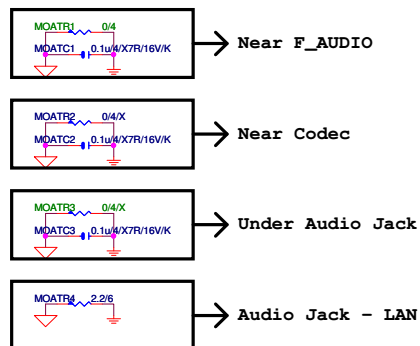
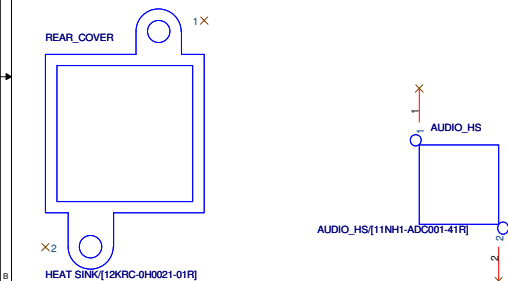
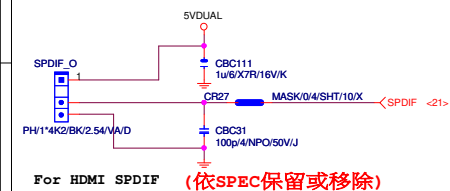
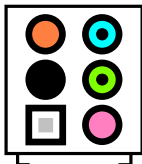
Title
ALC1220 CODECSize
Custom

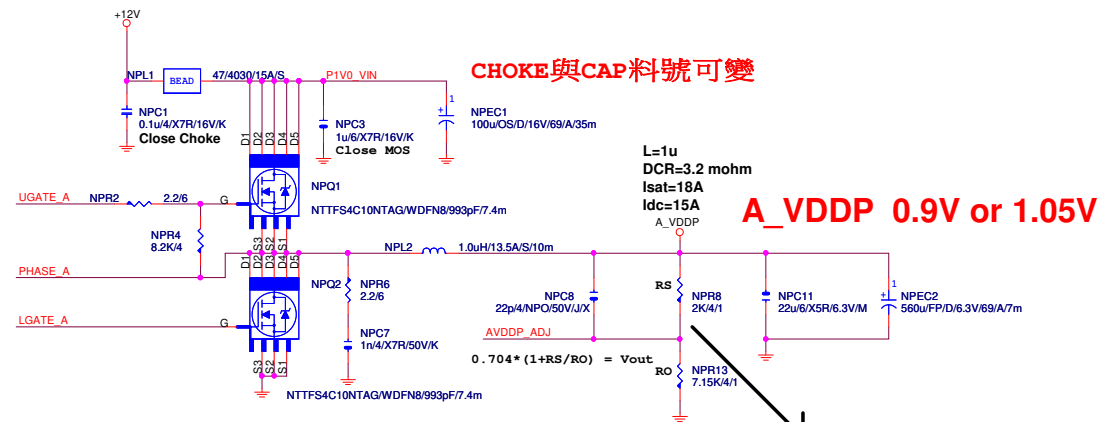
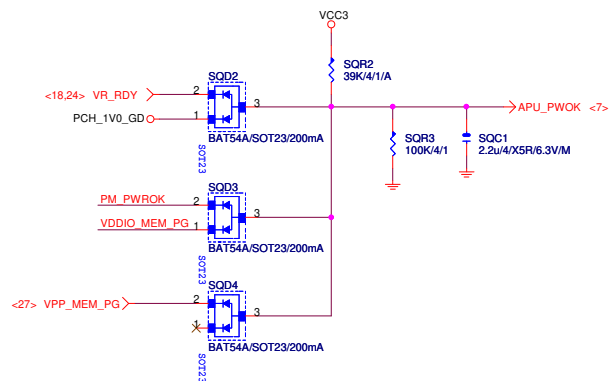
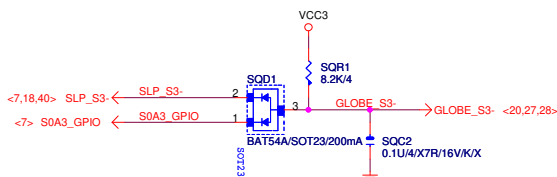
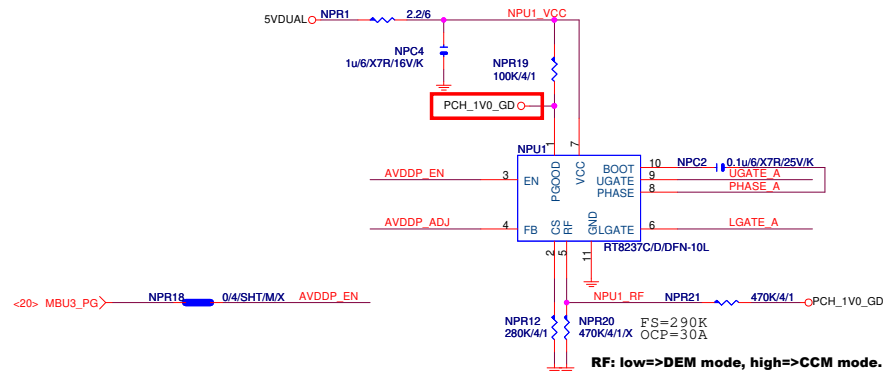
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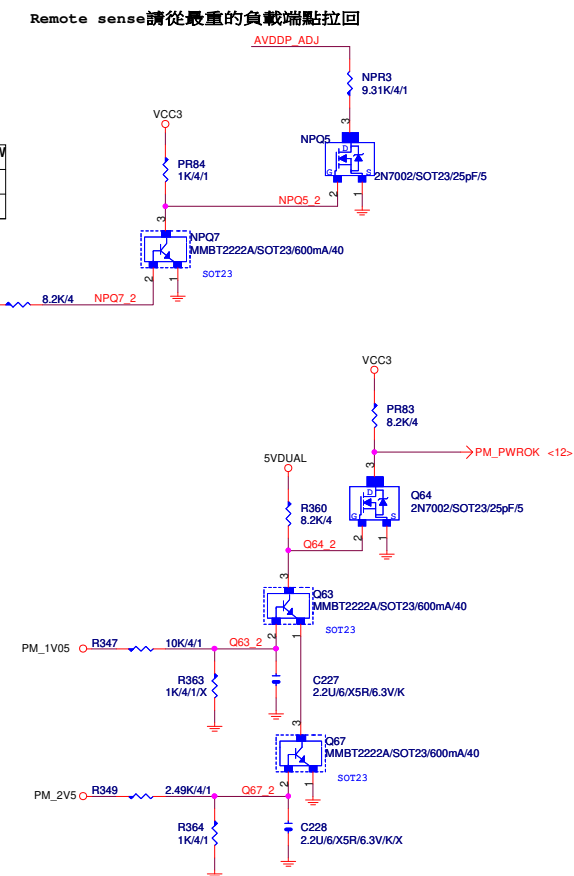
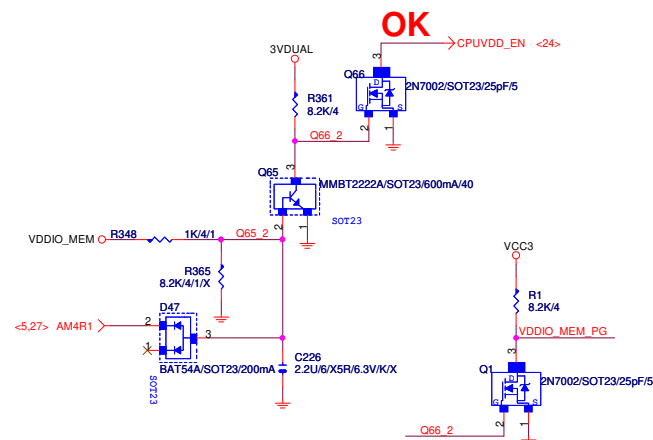
AZALIA JACK





CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

<5,20,37> CORETYPE1 PR85 8.2K/4 NPO7_2

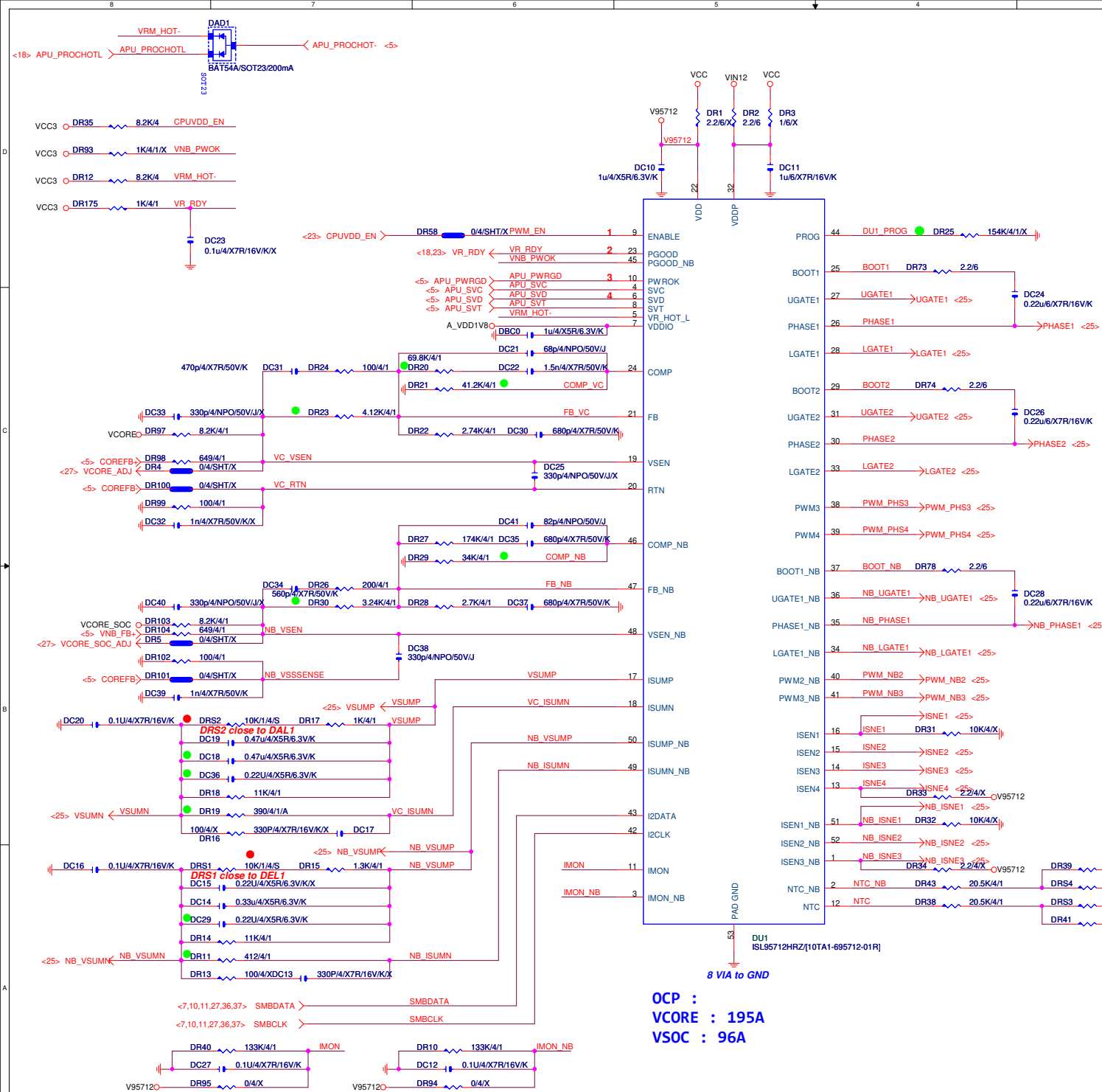


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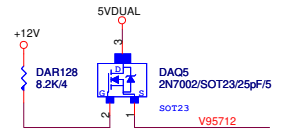
POWER SEQUENCE

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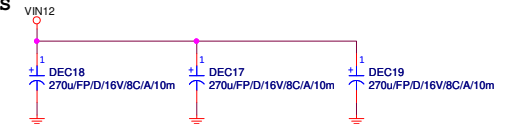
Date: Wednesday, August 19, 2020 Sheet 23 of B450 AORUS PRO



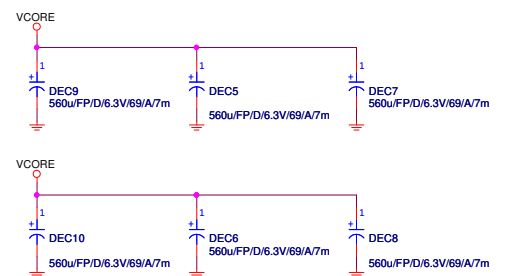
1. 新增DAR128.DAQ5 (12V負壓線路) 2. DR1改不上件



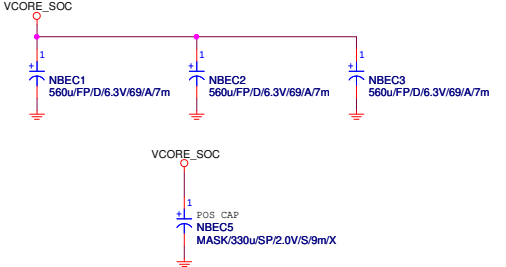
VIN * 3PCS



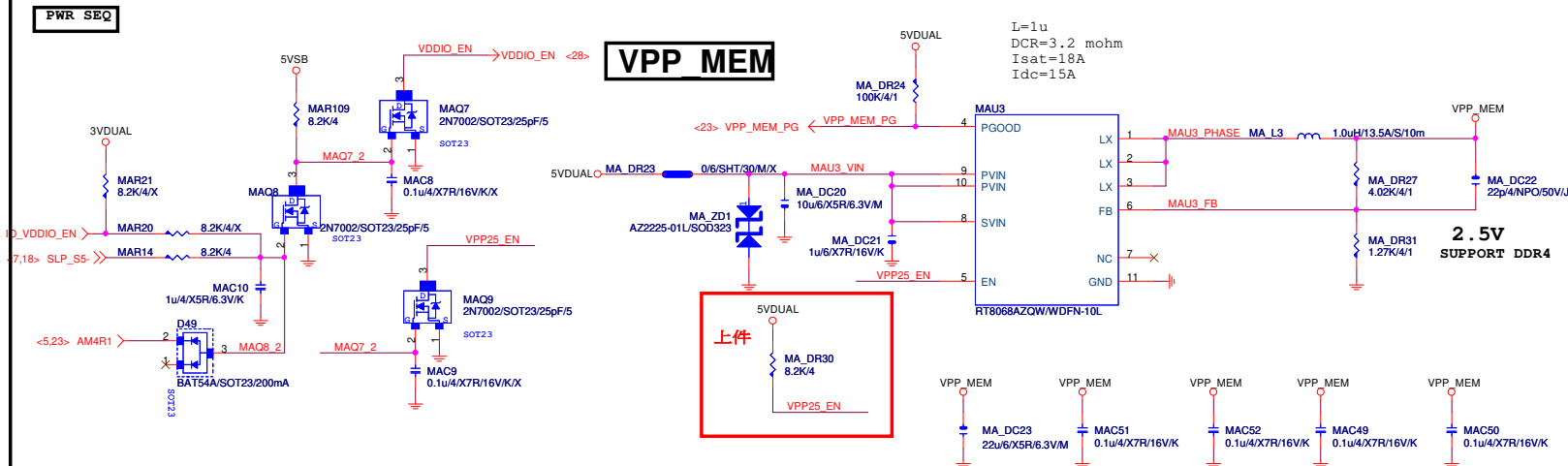
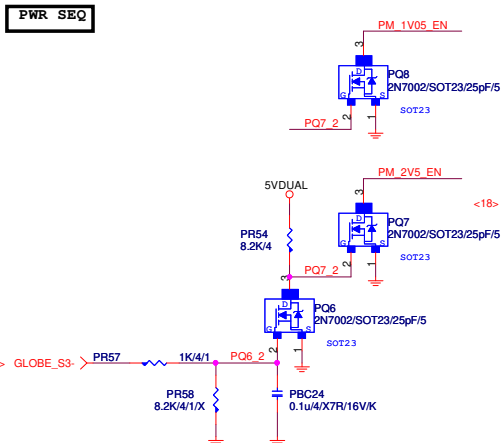
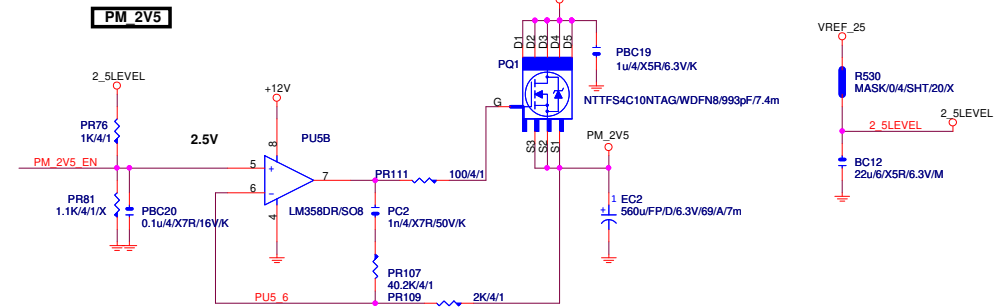
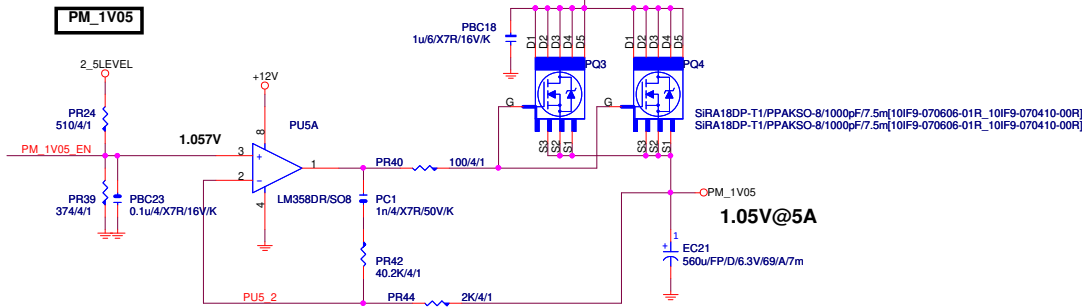
VCORE * 6 PCS



VSOC * 4 PCS



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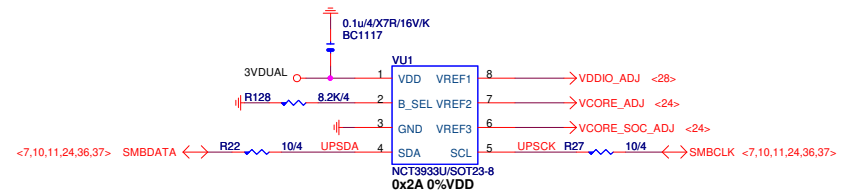


VDDCR SOC S5

S5_MUX: S0-->High, S5-->Low
H: VDDCR_SOC_S5 will track VCORE_SOC.
L: If VCORE_SOC < 0.775V (OR 0.85V) , VDDCR_SOC_S5=0.775V.
If VCORE_SOC>=0.775V (OR 0.85V) , VDDCR_SOC_S5 will trace VCORE_SOC.



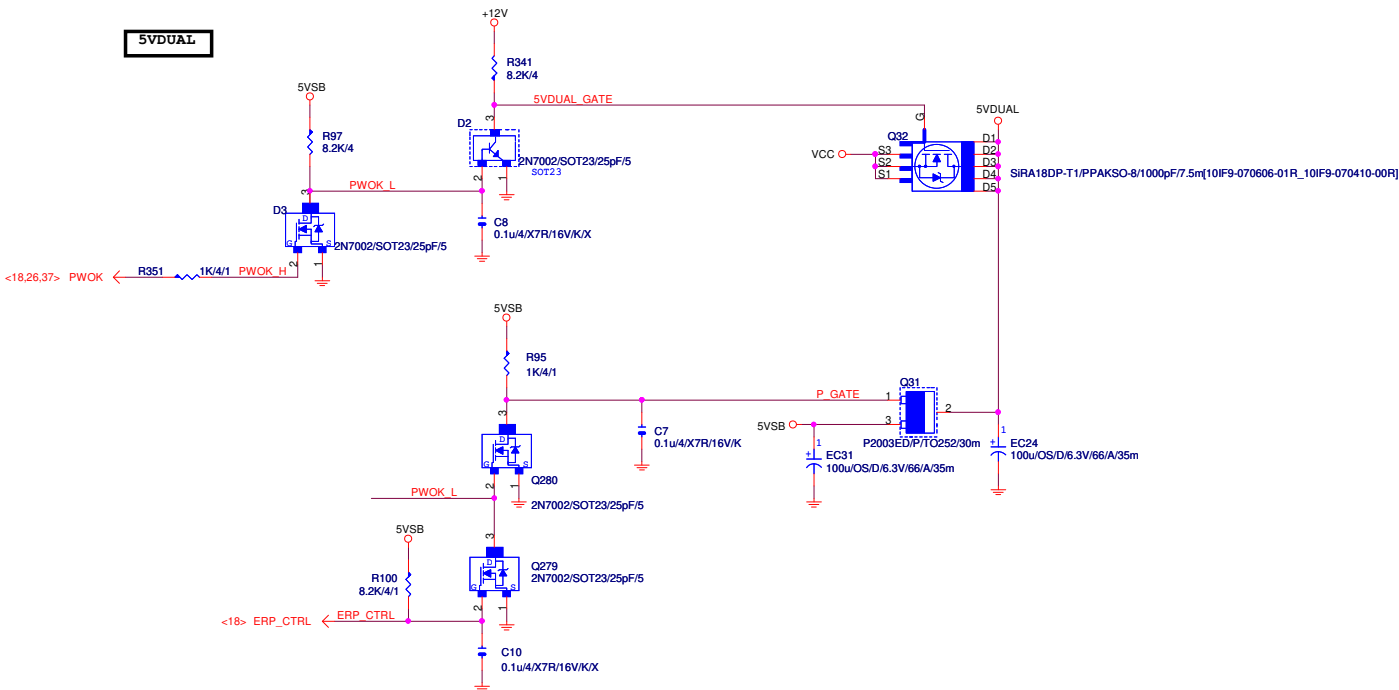
AM4 S5: 0.775V, 200mA,
S0:VAR, 900mA.



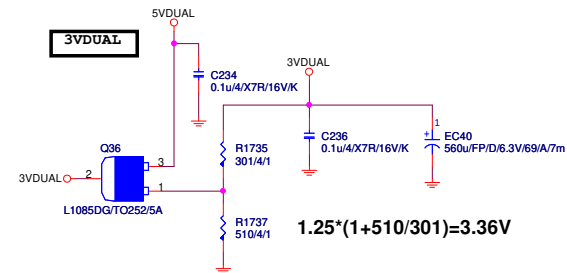
GIGABYTE

Title			
PM POWER			
Size	Document Number	Rev	
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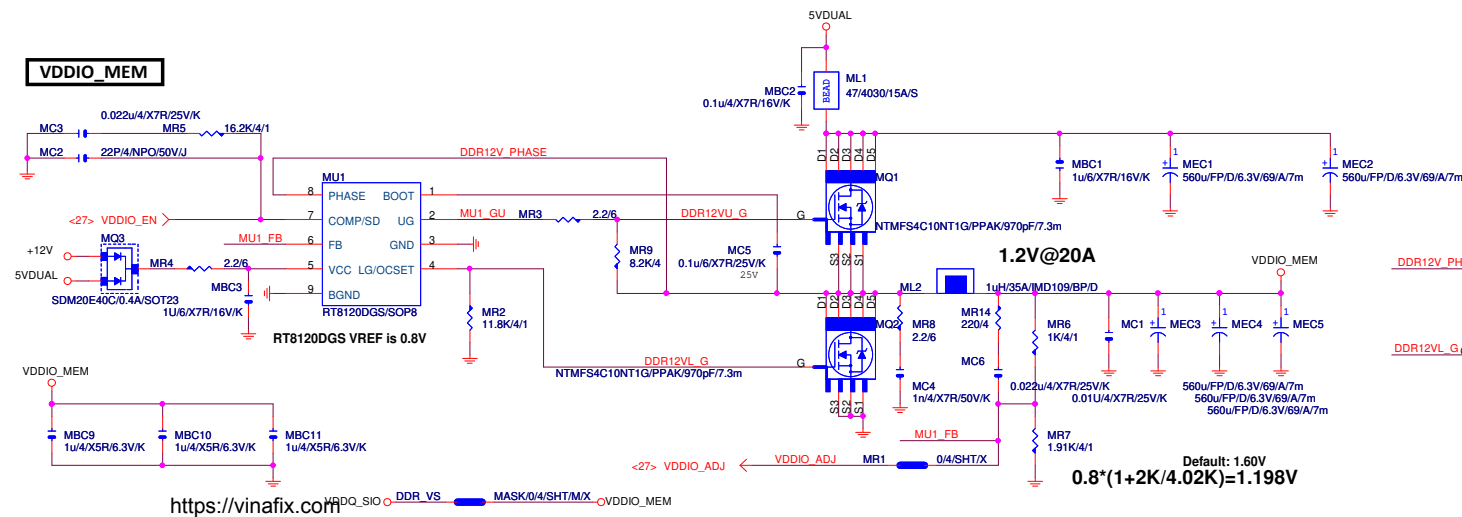
5VDUAL



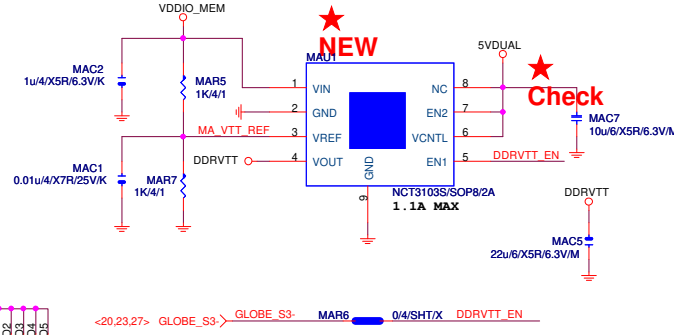
3VDUAL



VDDIO_MEM

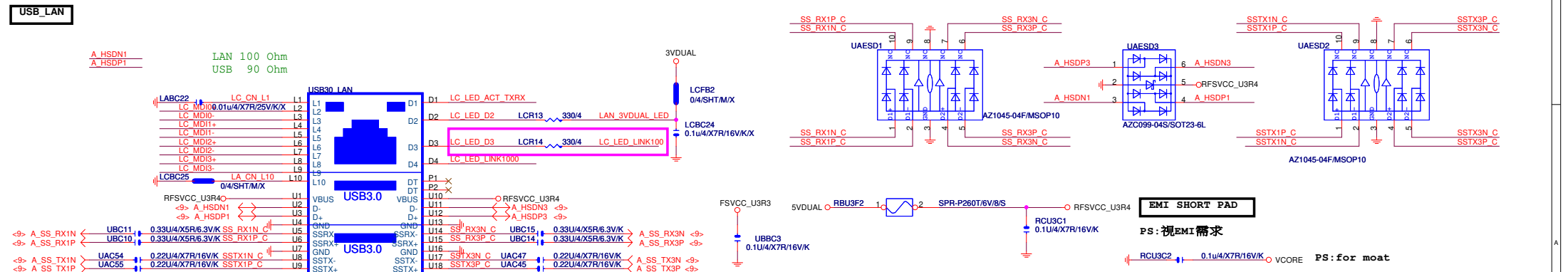
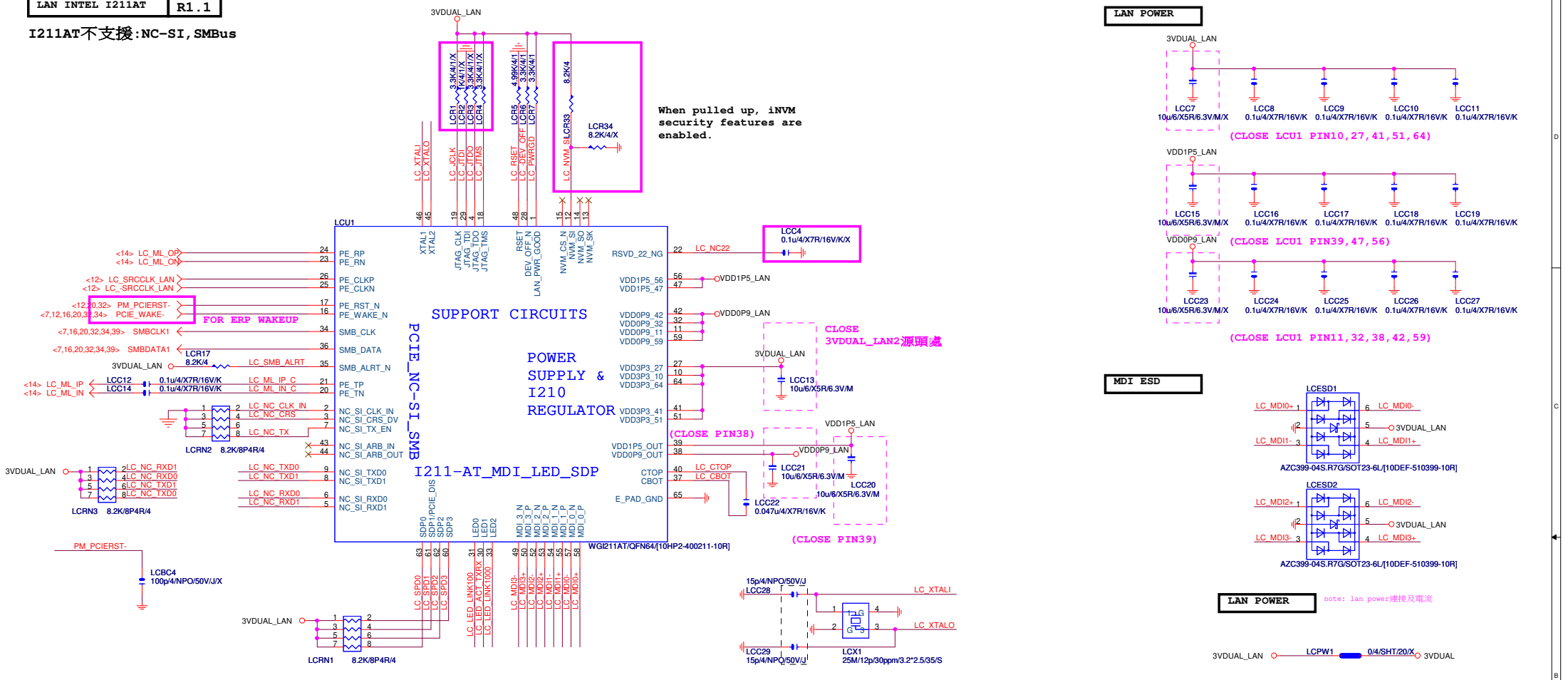


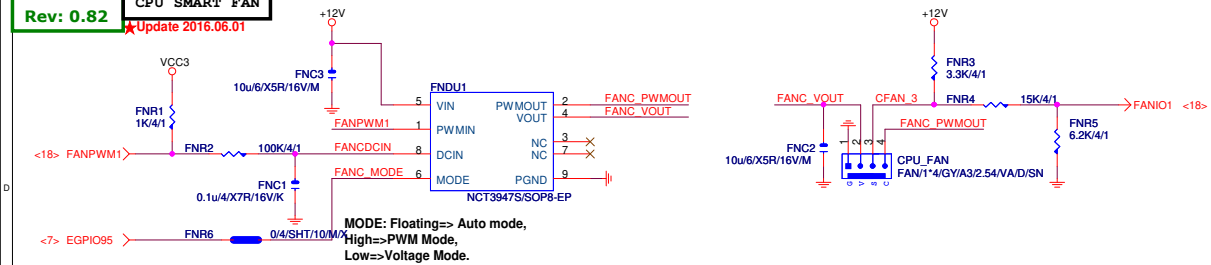
DDRVTT



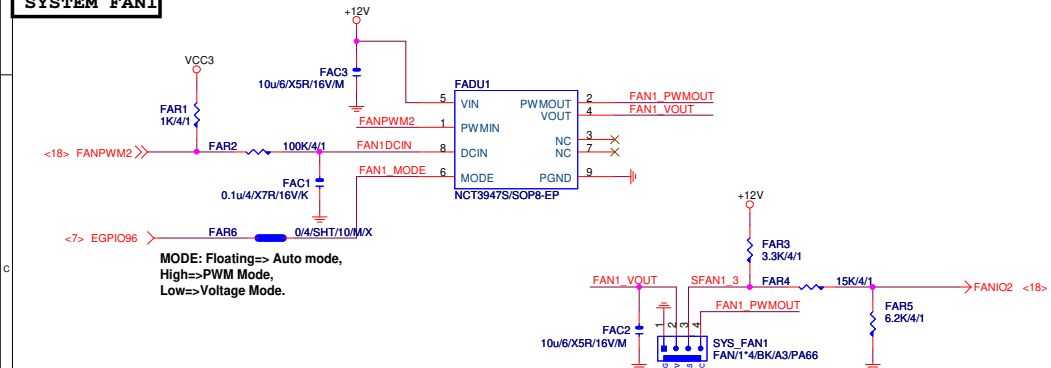
GIGABYTE

DDR PWR, 5VDUAL, 3VDUAL		
Size	Document Number	Rev
Custom	B450 AORUS PRO WIFI	1.1
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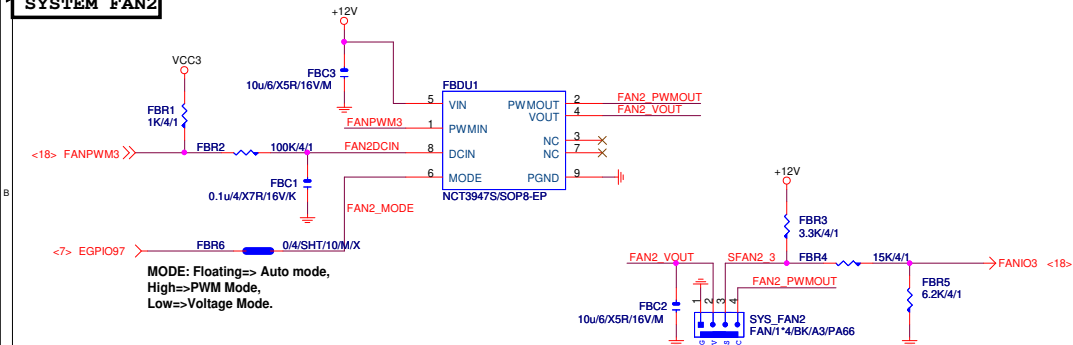




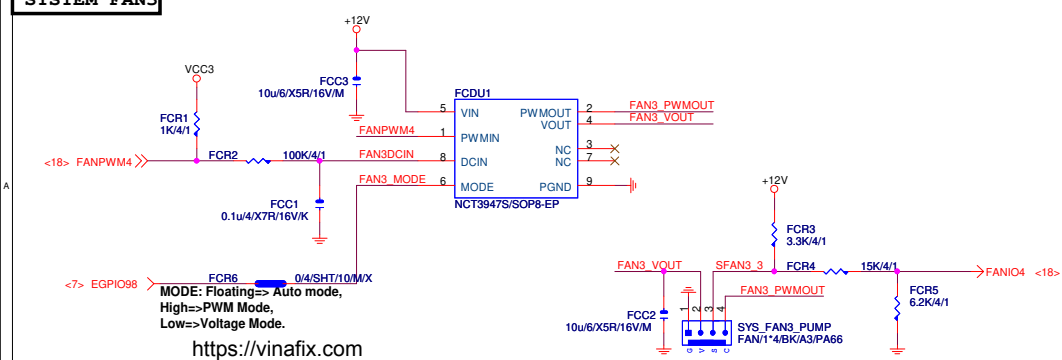
SYSTEM FAN1



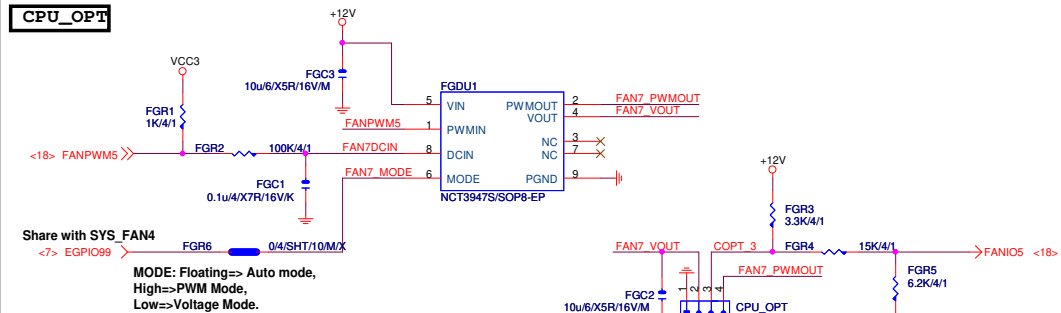
SYSTEM FAN2



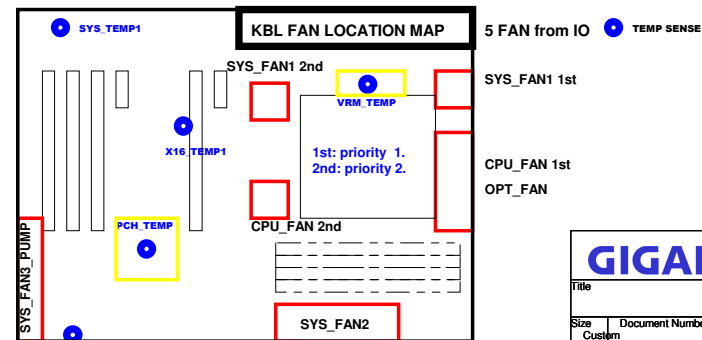
SYSTEM FAN3



CPU_OPT



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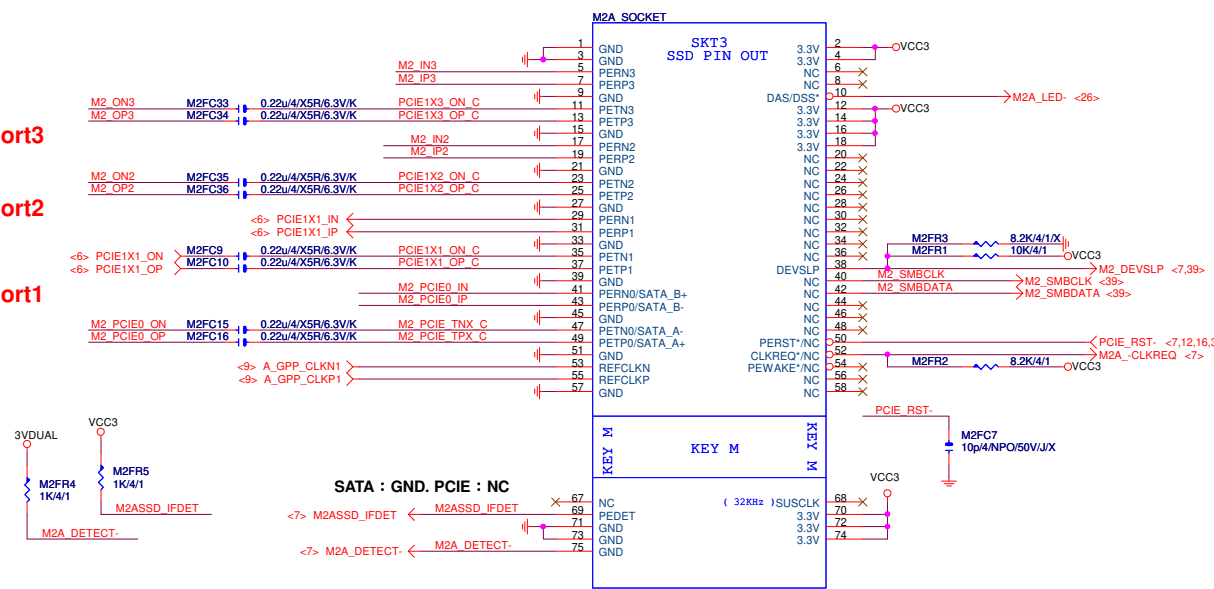
Rev 0.5

M.2 Lane4 from AM4 port3

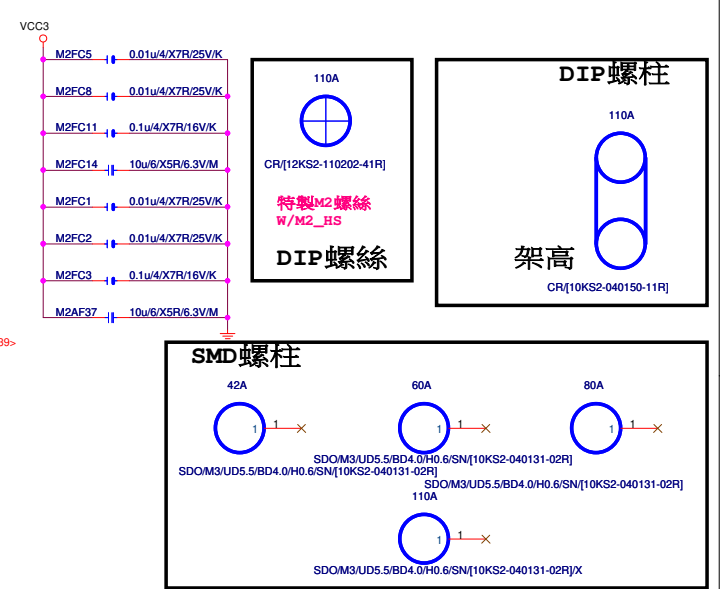
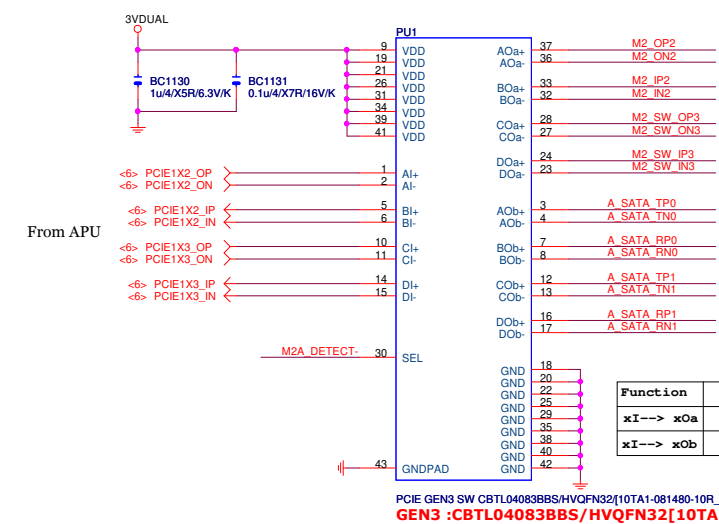
M.2 Lane4 from AM4 port2

M.2 Lane4 from AM4 port1

by SWITCH Select



8.5H鐵殼
Footprint :M2_110(DIP)

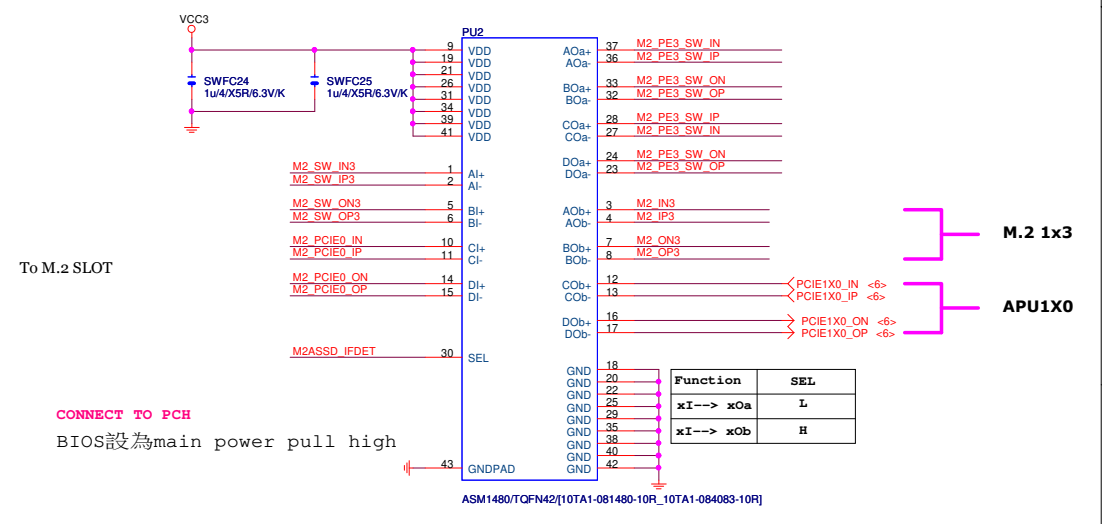
M2A_SOCKET
M2A_SOCKET_HS/[12SP1-S10205-32R_12SP1-S10205-33R] **M2 HEATSINK**

To M.2

TO SATA CONN

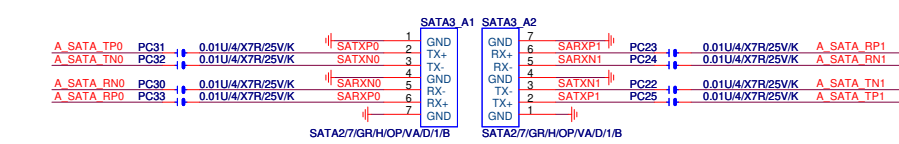


PCIE GEN3 SW CBTLO4083BBS/HVQFN32[10TA1-081480-10R_10TA1-084083-10R]
GEN3 :CBTLO4083BBS/HVQFN32[10TA1-084083-10R]



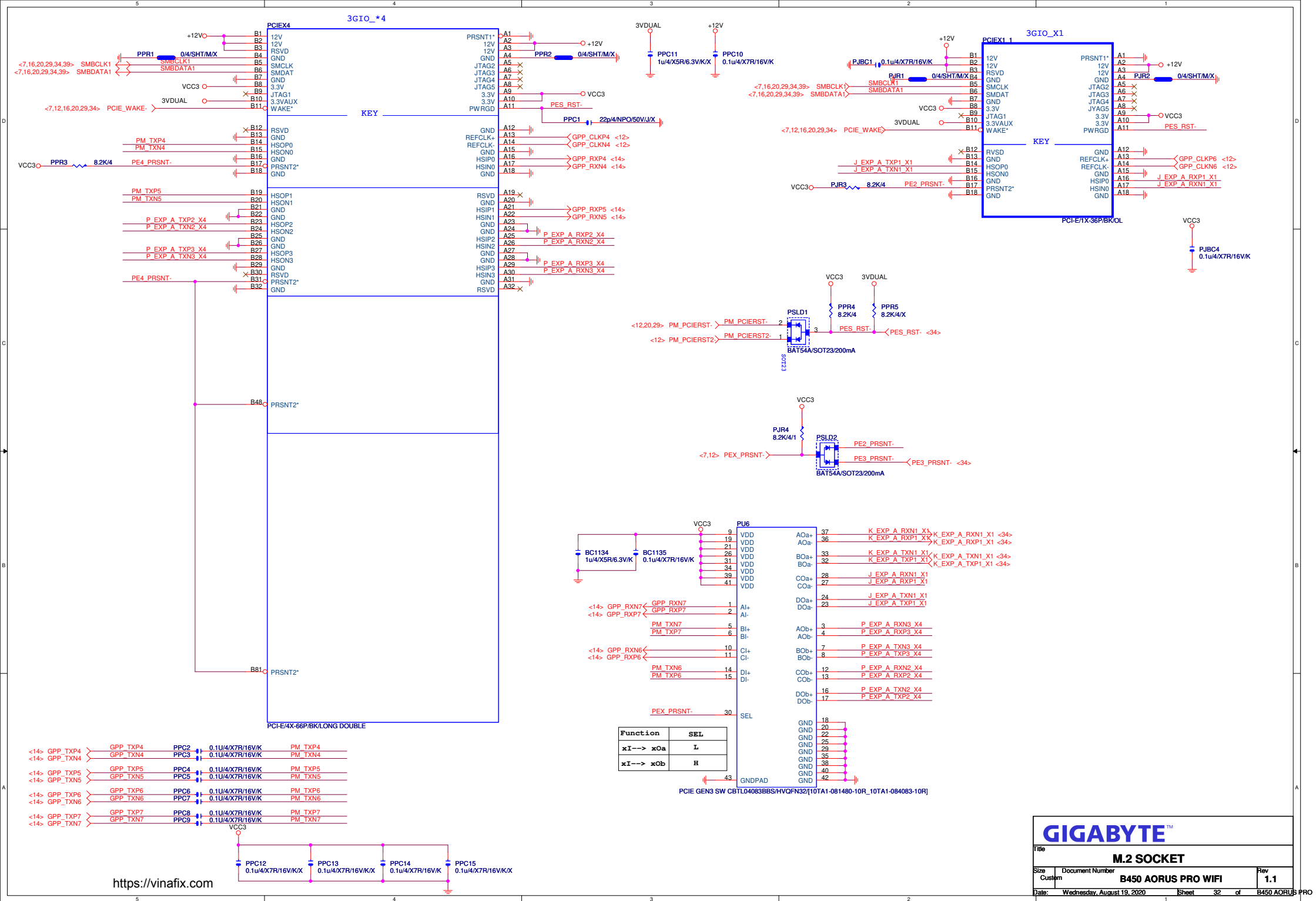
CONNECT TO PCH
BIOS設為main power pull high

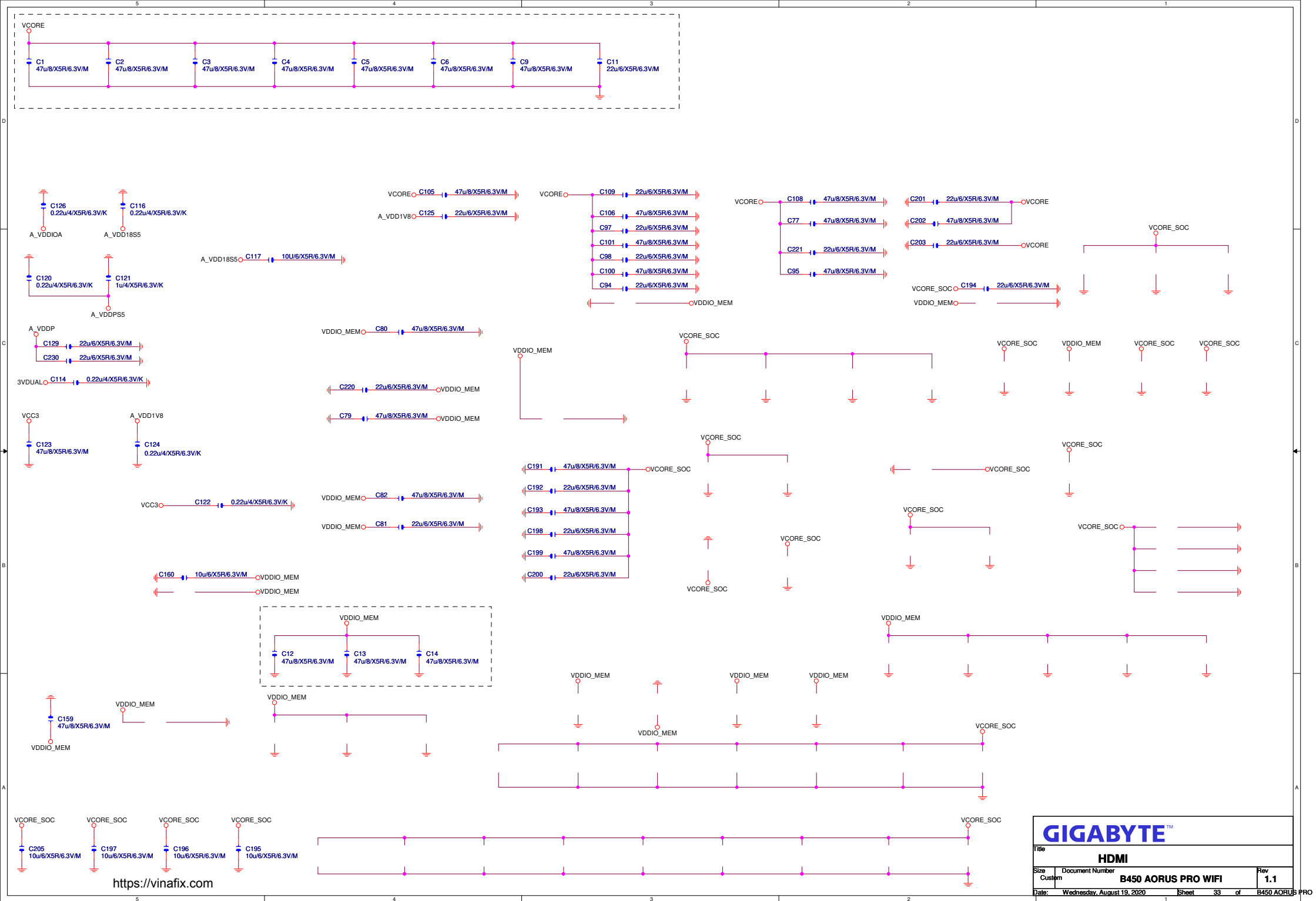
Function	SEL
xI--> xOa	L
xI--> xOb	H



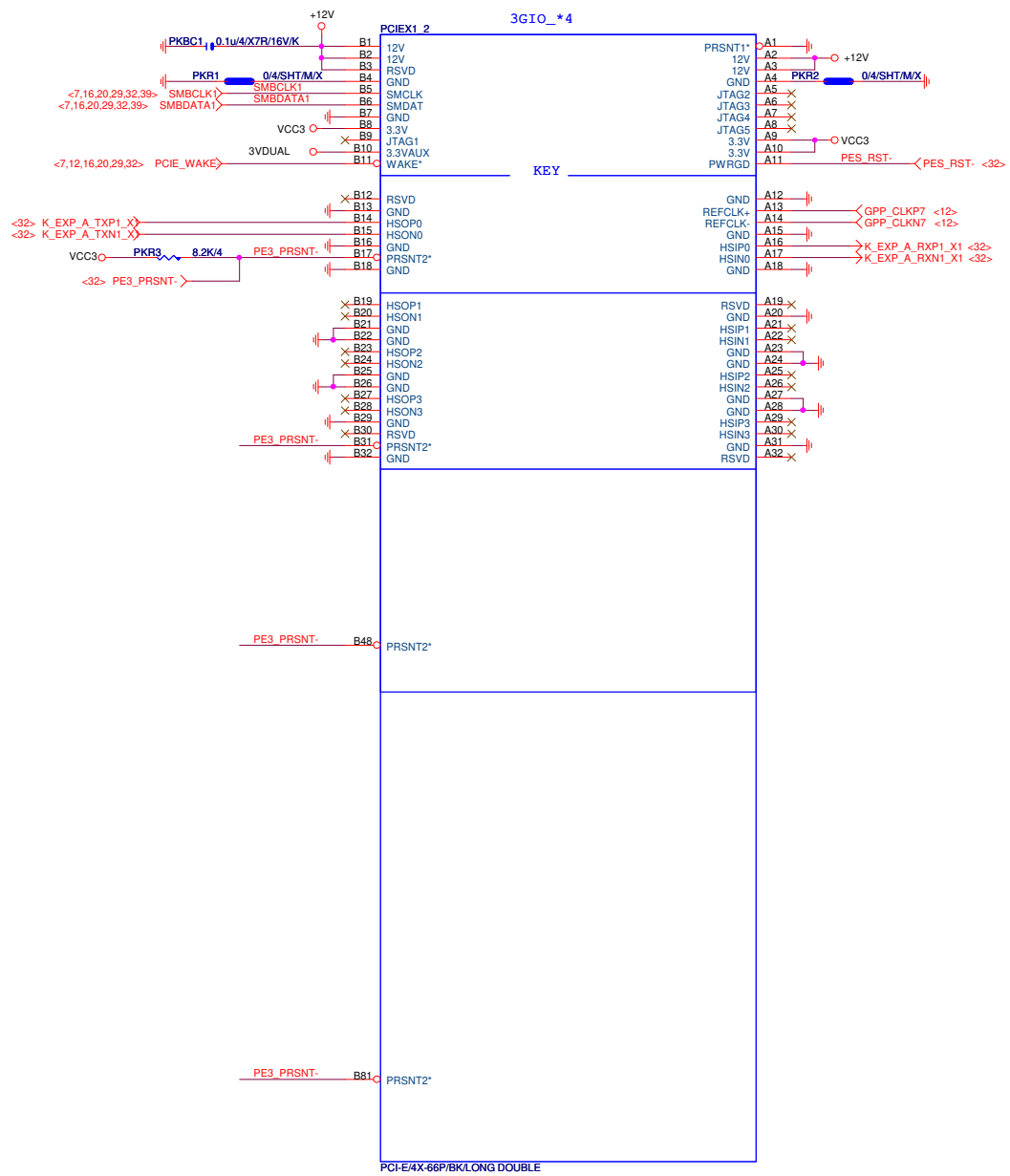
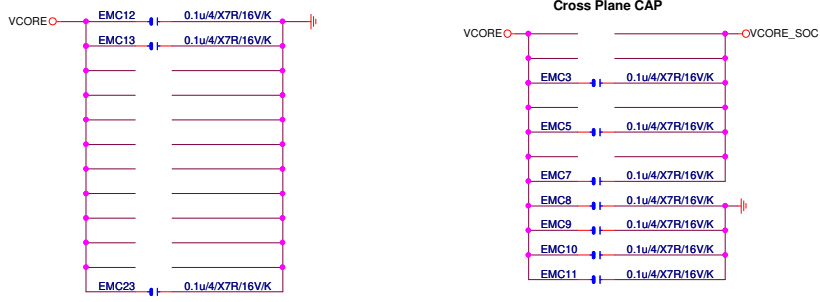
<https://vinafix.com>


GIGABYTE™			
Title M.2 SOCKET			
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CPU TOP CAVITY



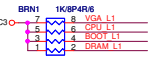
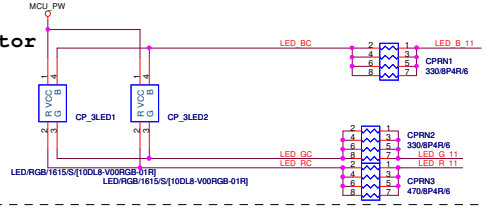
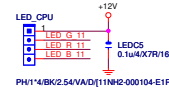
			
Title			
HDMI			
Size	Document Number	Rev	
Custom	B450 AORUS PRO WIFI	1.1	
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第一區 LED

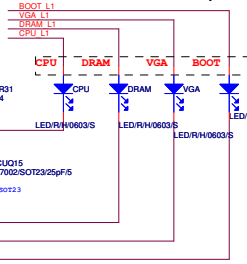
FOR CPU 正發光 LED*4
(在CPU CHOKe之間,MOS_HS下方,不外露)

FOR 裝甲高亮度 正發光 LED*2 (位置在正板,依據裝甲設計擺放)

AMD CPU_FAN LED connector



DEBUG PORT LED *4
(位置需擺放在一起)



用文字面表示

EC_GP71	CPU DEBUG
EC_GP72	DDR DEBUG
IO_GP63	VGA DEBUG
IO_GP64	BOOT DEVICE DEBUG
PM_GPIO6	software beat mode control
N_GPP_A22	
N_GPP_D12	

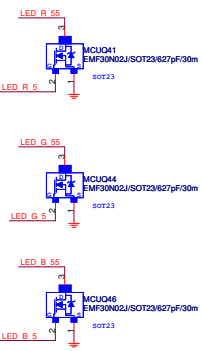
第二區 LED

FOR DIMM 側發光 LED*12
(位置在DIMM兩側)

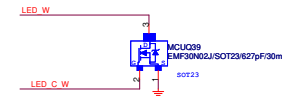
第五區 LED

燈條 LED (LED_C1放在PCB左邊板邊位置)

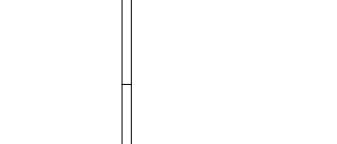
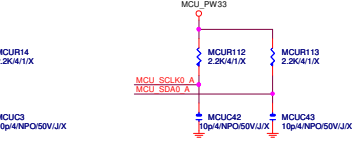
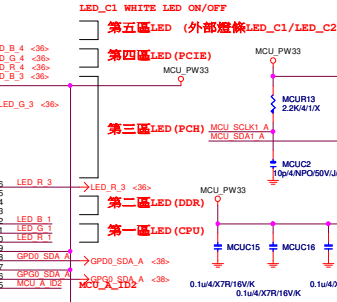
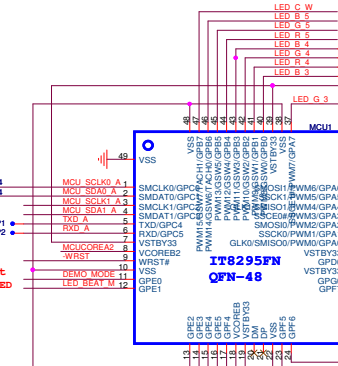
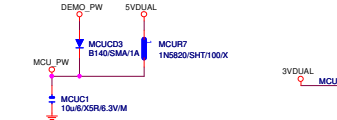
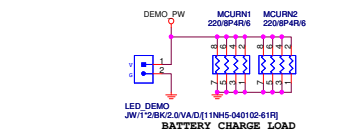
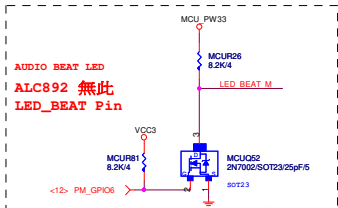
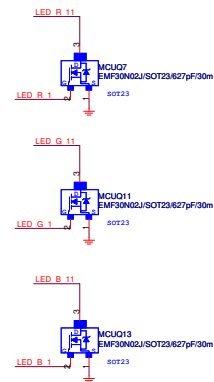
第五區 LED CONTROL



Footprint "PH1X5-ROW-L"



第一區 LED CONTROL



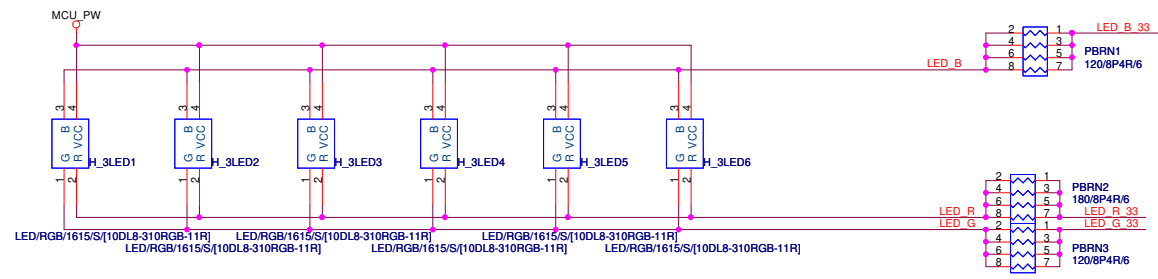
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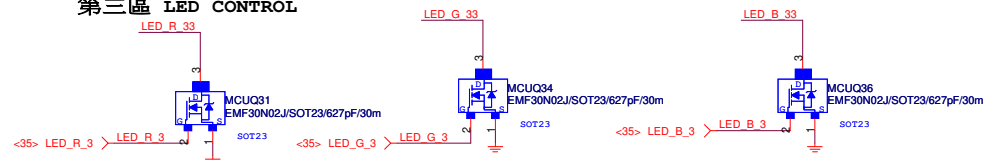
Title		CPU / AUDIO / PCIE/REAR LED	
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第三區 LED

FOR PCH 正發光 LED*6 (位置在正板, 依據PCH_HS設計擺放)



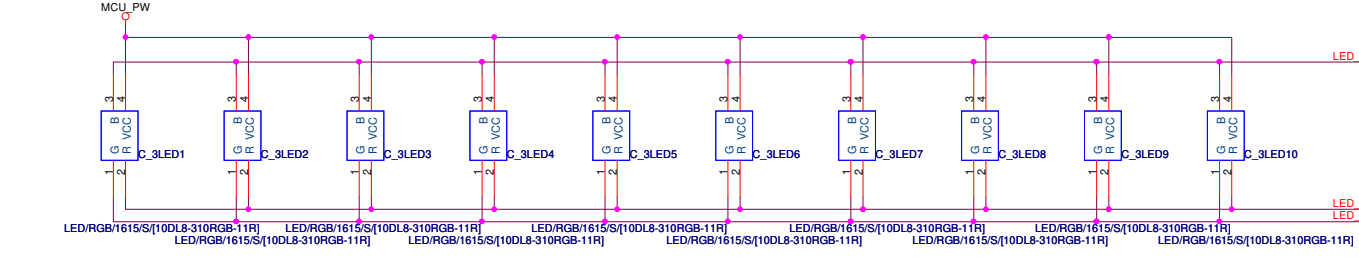
第三區 LED CONTROL



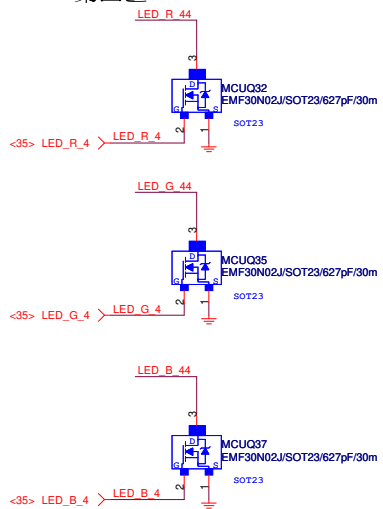
RGB LED壓克力燈條 REMOVE

第四區 LED

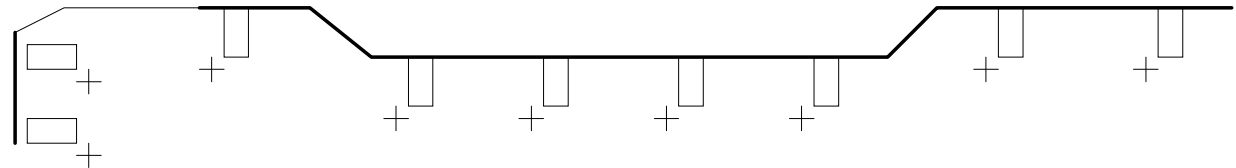
FOR AUDIO 正發光 LED*10 C_3LED1~10)



第四區 LED CONTROL



Audio Ground切割線+背面 RGB LED

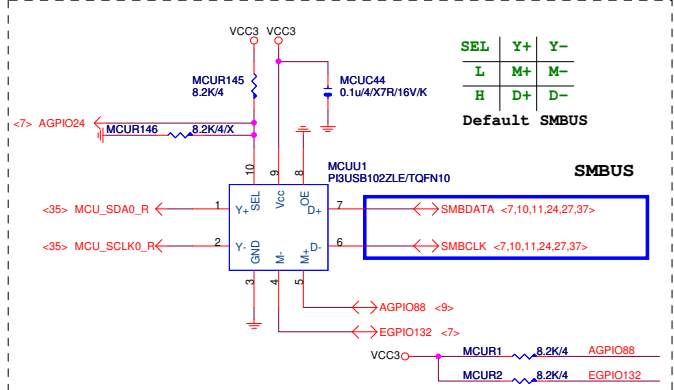


RGB LED LAYOUT 注意事項 :

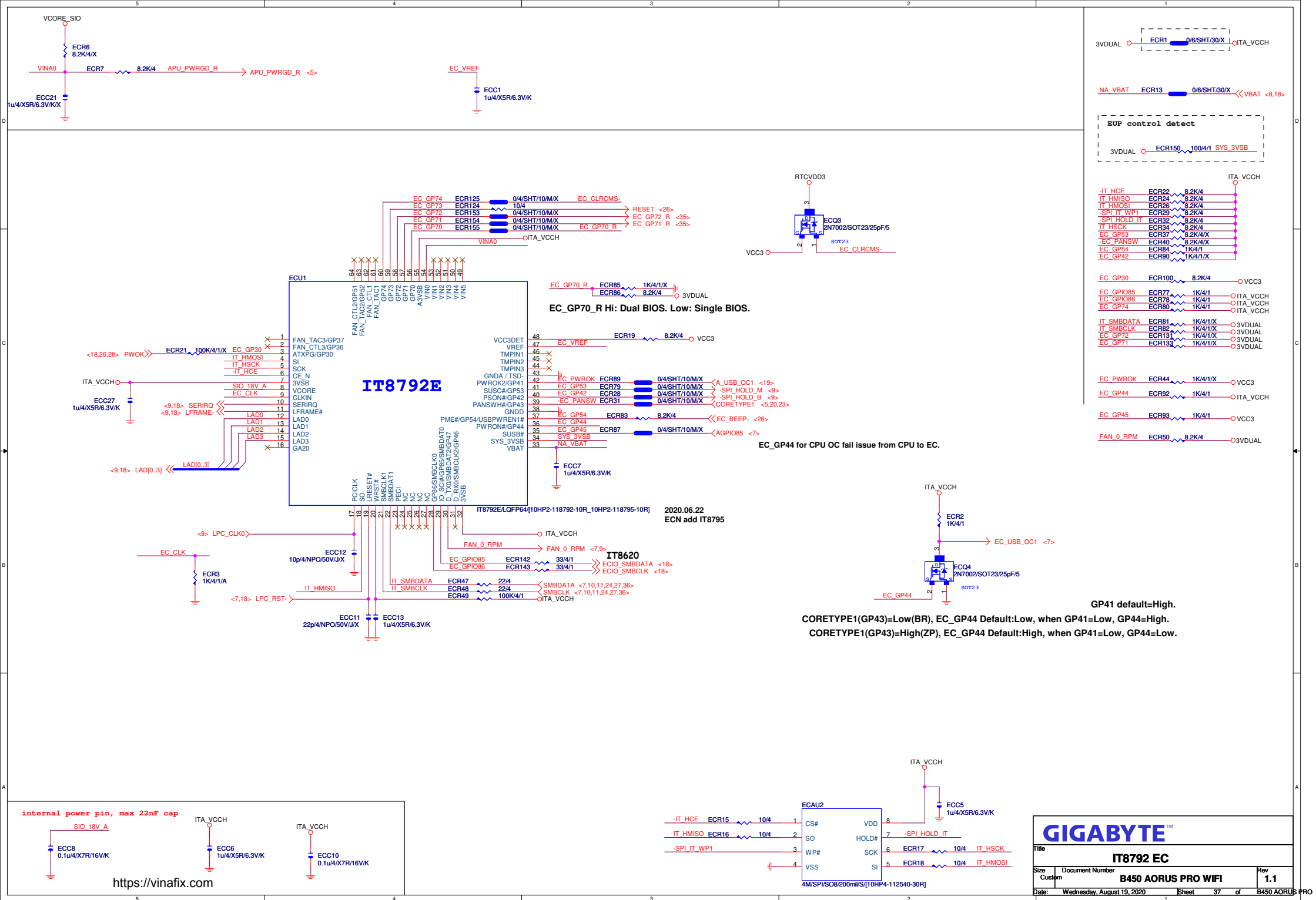
- 1. Debug LED (各LED依CPU/DRAM/VGA/BOOT個別位置擺放)
- 2. 背板 RGB LED 方向整板請統一如下 (整板正極可統一朝下或朝上)
- 3. 正板 RGB LED 統一方向即可
- 4. MCU_PW & MCU_PW33電源一律走20mils
- 5. ECF1, ECF2, ECF3, ECF5 兩端電源走80mils或用鋪銅方式加粗
- 6. MCU LED 出pin的走線4mils, 如: LED_R_1, LED_G_1, LED_B_1
- 7. LED RGBW rule : W/S=10/5 mils 如: LED_R_11, LED_G_11, LED_B_11, LED_W..... (包含從晶體到排阻到LED的net)
- 8. Digital LED NET rule W/S=4/8 mils GPD0_SDA_B, GPD0_SDA_BB, GPD0_SDA_C, GPD0_SDA_CC

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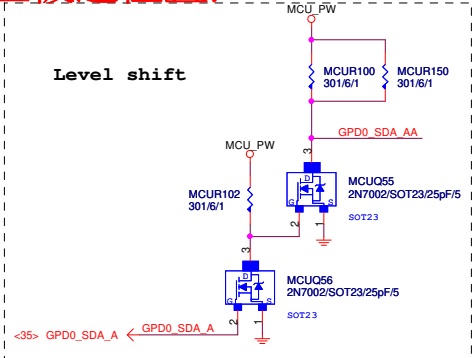
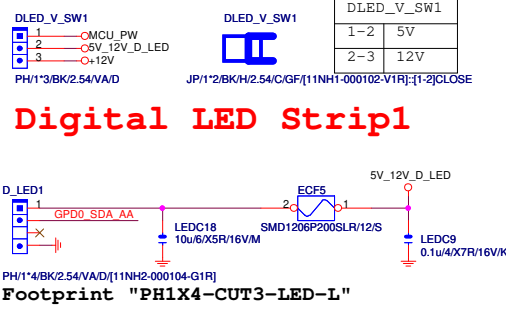
For AMD MCU update



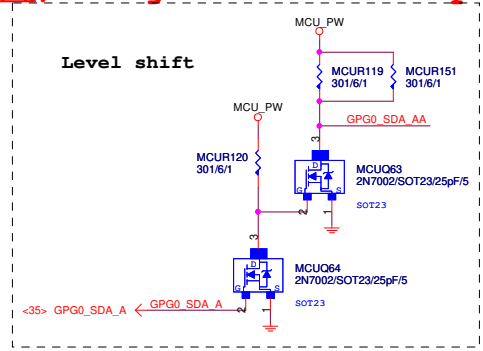
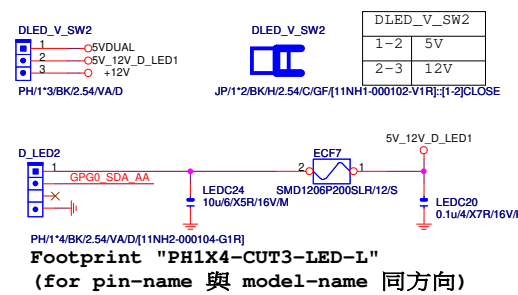
GIGABYTE
Title
PCB / PCH / DDR / LED_C LED
Size
Custom
Document Number
B450 AORUS PRO WIFI
Rev
1.1
Date: Wednesday, August 19, 2020
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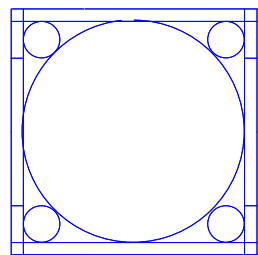
第六區 LED (靠近左上板邊位置)



第七區 LED (靠近右下DDR板邊位置) Digital LED Strip2

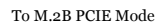


AIQ_SHIELD

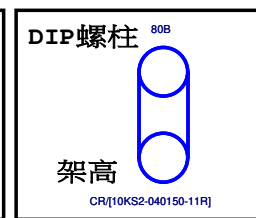


IO SH/SUS 4301-0.2mm AJOH0/[11AIO-0C0010-02R_11AIO-0C0010-22R]

Rev 0.5



Function	SEL
xI--> xOa	L
xI--> xOb	H



M2 HEATSINK

